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Nanosecond range pulse generators for quality control and diagnosis of Cherenkov telescope cameras

Generadores de pulso del orden de nanosegundos para control de calidad y diagnosis de las cámaras de telescopios Cherenkov

MEMORIA PARA OPTAR AL GRADO DE DOCTOR

PRESENTADA POR

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Doctoral Thesis written by

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A mi familia,

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SUMMARY

The main goal of this thesis consists in the development of compact nanosecond-range pulse generator technologies for the Cherenkov Telescope Array (CTA) project. The need of this work emerged during the development of the MAGIC II telescope, another Imaging Atmospheric Cherenkov Telescope (IACT) and a precursor of CTA.

This kind of instrument is used for detecting the Cherenkov radiation that has been generated by gamma rays when entering in contact with the atmosphere. Thus, reconstructing the shower axis in space and tracing it back onto the sky is possible to determine the cosmic source of the gamma-ray. The research of the VHE (very high energy) radiation allows obtaining significant information about the most energetic phenomena in the Universe.

The duration of the Cherenkov light is of about a few nanoseconds. As a consequence, the need for compact pulse generators emerged soon with the aim of testing the telescope acquisition chain. Additionally, they are required for performing both laboratory and field tests in several parts of the telescope, such as the camera photodetectors or the camera calibration.

Some of the applications demand a low size design since the pulser may be integrated in the telescope. As well, low cost is an essential feature in a project composed by a high number of institutes, where the expensive commercial pulse generators are not the best option. Finally, high accurate and reliability are critical factors to guarantee.

Despite all the applications mentioned above, it is believed that the scope of the work here presented is not restricted to CTA, but can be applied in a wide variety of other fields thanks to its versatility, compactness and reduced cost.

The first pulse generator here presented is based on Step Recovery Diodes (SRDs), which are characterized by their very abrupt turn off. The topology carried out consists in a pulse sharpener composed by the SRD, a short-circuited stub and a diode Schottky. Within this design pulses of more than 4 V amplitude and widths of the order of one nanosecond have been achieved. Additionally, a width jitter in the ps range has been obtained. As well it is worth to mention that the width of the pulses is simply controlled by just modifying the length of the stub, what provides with high versatility this pulse generator.

In particular, a four channel prototype has been developed for testing the receiver boards of MAGIC II telescope. In order to achieve identical waveforms it has been opted for splitting the output of the pulse generator, for which purpose a 4-way resistive divider has been used. As well, identical electrical lengths have been required in order to guarantee synchronized signals. Both characteristics (similarity and synchronization) are indispensable for detecting possible delays or other anomalies in the telescope acquisition chain.

Due to the loss of amplitude in the fan-out stage, the four channels have been next amplified. Two high gain and high bandwidth inverter amplifiers have been used per channel. Finally, a DC power board supplies the entire system. Low noise, low jitter and minimum ringing have been priority features along the development of each one of the stages that compose the prototype.

Thus, pulses of 4 V peak amplitude and 1.3 ns FWHM have been obtained at each channel, as required by the specifications. The prototype was successfully used for testing the receiver boards of the MAGIC II camera. Additionally, this design provided a basis for the development of a 96 fanout pulse generator which was successfully used for analyzing the readout system of the MAGIC upgrade, and it is proposed for testing the Dragon Boards of the CTA camera (CTA readout boards), which are based on the same chip.

Another topology of pulse generator has been proposed in this work, the Signal On Transition (SOT) pulser. In this design a control signal determines the path of a current source by the switching of four transistors. When it changes from high to low state or vice versa, and just in the middle of that transition, the current is driven throughout a specific path where a resistor has been placed. The voltage drop across the resistor produces the output pulse.

Next a matching stage has been developed, required for two reasons: 1) the outputs of the SOT circuit are inverted pulses baselined at the supply voltage, and 2) a high impedance load is needed. A design based on three high speed, low noise and low distortion operational amplifiers has been carried out. The two first act as buffers providing high impedance and load isolation. The third one is configured as a difference amplifier for filtering the DC signal and inverting the pulses, and has been carefully chosen to be able to provide high output current in order to achieve pulses of more than 4 V into a 50 ohms load.

The results obtained with the matching stage shows that the signal integrity is apparently preserved, something successful when designing high bandwidth matching networks from very high to low impedances. Thus, pulses of more than 4 V peak amplitude and less than 10 ns FWHM into a 50 ohms load have been achieved.

A special characteristic of this pulse generator is that the pulse width is controlled by means of the control signal slope, so in combination with the appropriate electronic it becomes a variable width pulse generator. With such aim a variable transition time control circuit (TTCC) has been developed, based on the charge and discharge of a capacitor by means of two variable current sources. In this design the rising and falling times are independently controlled by varying the value of the current sources, which is performed by means of potentiometers.

In this thesis the pulses obtained with the SRD generator have been slightly the narrowest and the most stable. Nevertheless, it is expected to improve to a great extent the characteristics of the pulses achieved with the SOT generator by carrying out a circuit integrated implementation and using more stable current sources.

Additionally, the SOT pulse generator presents some special features that become it in a very useful and versatile tool. Apart from the above mentioned possibility of modifying the pulse width, opposite to the SRD pulser where each board is designed for a particular width, it is also possible to activate/deactivate the pulses when required by just enabling/disabling the SOT circuit current source. That allows creating any desired pulse pattern.

Furthermore, replacing the analog potentiometers that determine the control signal slope by digital ones and adding the digital circuitry necessary for managing the SOT circuit current source (e.g. a transistor for turning on and off the current source) allows it to be remotely controlled by a computerized system. Thus, a new branch of application in automation processes is opened.

In conclusion, it is believed to have shown the high potential of the pulse generators presented in this thesis. Besides the successful use of the prototypes developed, these pulsers could also be used in tests within the verification and validation (V&V) processes of CTA, which are not definitively defined at the time of writing this thesis. Additionally, due to their versatility, compactness and low cost they can be used in a wide variety of other applications.

RESUMEN

El principal objetivo de esta tesis consiste en el desarrollo de generadores de pulsos del orden de nanosegundos con la finalidad de ser utilizados en el proyecto CTA (Cherenkov Telescope Array). La necesidad de este trabajo surgió durante el desarrollo del telescopio MAGIC II, otro telescopio de espejo IACT (Imaging Atmospheric Cherenkov Telescope) y precursor de CTA.

Este tipo de instrumento se utiliza para detectar radiación Cherenkov que ha sido generada por rayos gamma cuando entran en contacto con la atmosfera. Así, reconstruyendo el eje de la cascada de partículas en el espacio y rastreando su origen hacia el cielo es posible conocer la fuente cósmica de los rayos gamma. El estudio de la radiación de muy alta energía (VHE) permite obtener información muy relevante acerca de los procesos más energéticos que tienen lugar en el Universo.

La duración de la radiación Cherenkov es de tan sólo unos pocos nanosegundos. Como consecuencia de esto la necesidad de generadores de pulsos compactos emergió con la finalidad de testear la cadena de adquisición del telescopio. Asimismo también son necesarios para realizar ensayos tanto de laboratorio como de campo de diferentes partes del telescopio, tales como los fotodetectores de la cámara o la calibración de la misma.

Algunas de las aplicaciones requieren de un tamaño reducido ya que el generador de pulsos puede ir integrado en el telescopio. Asimismo, un bajo coste es una característica fundamental en un proyecto formado por un elevado número de instituciones, donde los generadores de pulsos comerciales no son la mejor opción debido a su elevado precio. Por último, un alto grado de precisión y fiabilidad son factores críticos que garantizar.

A parte de las aplicaciones mencionadas, se cree que el alcance del trabajo aquí presentado no se limita a CTA, sino que puede aplicarse en una amplia variedad de campos gracias a su versatilidad, compacidad y bajo coste.

El primer generador de pulsos que se presenta está basado en diodos SRD (Step Recovery Diodes), los cuales se caracterizan por presentar transiciones de conducción a corte muy abruptas. La topología llevada a cabo consiste en un conformador de pulsos compuesto de un SRD, un stub cortocircuitado y un diodo Schottky. Con este diseño se han conseguido pulsos de más de 4 V de amplitud y anchos del orden de un nanosegundo. Además, se ha obtenido un jitter del ancho de los pulsos del orden de picosegundos. Asimismo merece la pena destacar que el ancho de los pulsos se controla con tan sólo modificar la longitud del stub, lo que le confiere una elevada versatilidad a este generador.

En particular se ha desarrollado un prototipo de cuatro canales para testear las placas receptoras del telescopio MAGIC II. Con el fin de conseguir formas de onda idénticas se ha optado por dividir la salida del generador de pulsos, para lo cual se ha utilizado un

divisor resistivo de 4 vías. Asimismo, se han requerido longitudes eléctricas idénticas para garantizar señales sincronizadas. Ambas características (similitud y sincronización) son indispensables para poder detectar posibles retrasos u otras anomalías en la parte de adquisición del telescopio.

Debido a la pérdida de amplitud en la etapa de división, los cuatros canales se han amplificado a continuación. Para ello se han utilizado por cada canal dos amplificadores inversores de alta ganancia y alto ancho de banda. Por último, una placa de alimentación DC suministra tensión a todo el sistema. Bajo ruido, bajo jitter y mínimo ringing han sido características prioritarias a lo largo del desarrollo de cada una de las etapas que componen el prototipo.

De esta manera se han obtenido pulsos de 4 V de amplitud de pico y anchos de 1.3 ns FWHM en cada canal, tal y como requerían las especificaciones. El prototipo se utilizó satisfactoriamente para testear las placas receptoras de la cámara del MAGIC II. Además, este diseño sirvió de base para el desarrollo de un generador de pulsos de 96 canales que fue empleado con éxito para analizar el sistema de lectura de la actualización de MAGIC, y que se propone para testear las “Dragon Boards” de la cámara de CTA (las placas de lectura de CTA), las cuales se basan el mismo chip.

En este trabajo se ha propuesto otra topología de generador de pulsos, el generador SOT (Signal On Transition). En este diseño una señal de control determina el recorrido de una fuente de corriente mediante la conmutación de cuatro transistores. Cuando cambia de estado alto a bajo o viceversa, y exclusivamente en mitad de la transición, la corriente es conducida a través de un camino específico en el cual se ha situado una resistencia. El voltaje a través de esta resistencia origina el pulso de salida.

A continuación se ha desarrollado una red de adaptación, la cual es necesaria por dos motivos: 1) las salidas del generador SOT son pulsos invertidos referenciados al voltaje de alimentación, y 2) se requiere una carga que presente alta impedancia. Se ha llevado a cabo un diseño basado en tres amplificadores operacionales de alta velocidad, bajo ruido y baja distorsión. Los dos primeros actúan como buffers proporcionando alta impedancia y aislamiento de la carga. El tercero se configura como amplificador restador para filtrar la señal DC e invertir los pulsos, y ha sido cuidadosamente seleccionado para ser capaz de suministrar una alta corriente de salida con el fin de conseguir pulsos de más de 4 V para una carga de 50 ohms.

Los resultados obtenidos con la etapa de adaptación muestran que la integridad de la señal aparentemente se preserva, lo cual representa un éxito cuando se diseñan redes de adaptación de alta a baja impedancia y de gran ancho de banda. Se han obtenido así pulsos de más de 4 V de amplitud de pico y menos de 10 ns FWHM para una carga de 50 ohms.

Una característica especial de este generador de pulsos es que el ancho del pulso se controla mediante la pendiente de la señal de control, por lo que en combinación con la electrónica apropiada se convierte en un generador de pulsos de anchos variables. Con tal

objetivo se ha desarrollado un circuito de control con tiempos de transición variables (TTCC), el cual se basa en la carga y descarga de un condensador a través de dos fuentes de corriente variables. En este diseño los tiempos de subida y bajada se controlan de manera independiente modificando el valor de las fuentes de corriente, lo cual se realiza mediante potenciómetros.

En esta tesis los pulsos obtenidos con el generador SRD han sido ligeramente los más estrechos y los más estables. Sin embargo se espera que las características de los pulsos obtenidos con el generador SOT mejoren en gran medida llevando a cabo una implementación en circuito integrado y utilizando fuentes de corriente más estables.

Asimismo, el generador de pulsos SOT presenta ciertas características especiales que lo convierten en una herramienta muy útil y versátil. Aparte de la ya mencionada posibilidad de modificar el ancho de los pulsos, al contrario que en el generador SRD donde cada placa se diseña para una anchura en particular, también es posible activar/desactivar los pulsos cuando se requiera con solamente habilitar/deshabilitar la fuente de corriente del circuito SOT. Esto permite crear cualquier patrón de pulsos deseado.

Además, reemplazando los potenciómetros analógicos que determinan la pendiente de la señal de control por unos digitales y añadiendo la circuitería digital necesaria para controlar la fuente de corriente del circuito SOT (por ejemplo un transistor para activar y desactivar la fuente de corriente) permite que éste sea controlado de manera remota por un sistema computarizado. Se abre así una nueva rama de aplicación en los procesos de automatización.

Como conclusión, se cree haber mostrado el alto potencial de los generadores de pulsos presentados en esta tesis. Aparte de la utilización con éxito de los prototipos desarrollados, estos generadores podrían emplearse también en ensayos de los procesos de verificación y validación (V&V) de CTA. Asimismo, gracias a su versatilidad, compacidad y reducido coste pueden utilizarse en una amplia variedad de otras aplicaciones.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

List of Tables

ABBREVIATIONS

ADC	Analog to Digital Converter
AMC	Active Mirror Control
ASIC	Application Specific Integrated Circuit
ASPERA	AStroParticle ERAnet
BERT	Bit Error Rate Tester
CBCPW	Conductor-Backed Coplanar Waveguide
CF	Carbon Fiber
CFRP	Carbon-Fiber-Reinforced Polymer
CTA	Cherenkov Telescope Array
CTF	Camera Test Facilities
DAQ	Data Acquisition
DJ	Deterministic Jitter
DRS	Domino Ring Sampler
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESFRI	European Strategy Forum on Research Infrastructures
FEXT	Far End Crosstalk
FPGA	Field Programmable Gate Array
FPI	Focal Plane Instrumentation
FWHM	Full Width at Half Maximum
GR	Generation-Recombination
HBT	Heterojunction Bipolar Transistor
HV	High Voltage
IACT	Imaging Atmospheric Cherenkov Telescope

IC	Integrated Circuit
IFAE	Institut de Fisica d'Altes Energies (Barcelona)
INFN	Istituto Nazionale di Fisica Nucleare
IP	Ingress Protection
JFET	Junction Field Effect Transistor
JNF	Jitter Noise Floor
LED	Light Emitting Diode
LST	Large Size Telescope
LVDS	Low-Voltage Differential Signaling
MMIC	Microwave Monolithic Integrated Circuit
MoU	Memorandum of Understanding
MST	Medium Size Telescope
MUX-FADC	Multiplexed Flash Analog-to-Digital Converter
NASA	National Aeronautics and Space Administration
NEXT	Near End Crosstalk
NLTL	Non-linear Transmission Line
NMOS	N-channel Metal Oxide Semiconductor
NRZ	Non Teturn-to-Zero
NSB	Night Sky Background
OPAMP	Operational Amplifier
PACTA	PreAmplifier for the CTA camera
PCB	Printed Circuit Board
PMOS	P-channel Metal Oxide Semiconductor
PMT	Photomultiplier Tube
QE	Quantum Efficiency
RAMS	Reliability, Availability, Maintainability and Safety

RF	Radio Frequency
RJ	Random Jitter
RMS	Root Mean Squares
RTS	Random Telegraph Signal
SCB	Slow Control Board
SCT	Schwarzschild-Couder Telescope
SiPM	Silicon Photomultiplier
SNR	Signal to Noise Ratio
SOT	Signal On Transition
SRD	Step Recovery Diode
SSO	Simultaneous Switching Outputs
SST	Small Size Telescope
TD	Tunnel Diode
TDC	Time to Digital Converter
TEM	Transverse Electromagnetic
TIE	Time interval error
TTCC	Transition Time Control Circuit
TTL	Transistor–Transistor Logic
UCM	Universidad Complutense de Madrid
UV	Ultraviolet
UWB	Ultra Wide-Band
V&V	Validation and Verification
VCSEL	Vertical Cavity Surface Emitting Laser
VHE	Very High-Energy
VME	Versa Module Europa

Introduction

Motivation

The main goal of this thesis consists in the development of compact nanosecond-range pulse generator technologies for the Cherenkov Telescope Array (CTA) project. The need of this work emerged during the development of the MAGIC II telescope, another Cherenkov telescope and a precursor of CTA. These instruments are called Imaging Atmospheric Cherenkov Telescopes (IACTs) and are able to provide information from distant galactic and extragalactic sources by detecting Cherenkov radiation cascades in the atmosphere, which are extremely faint and short, in the range of a few nanoseconds. As a consequence, the development of the instrumentation needs the use of compact pulse generators in a number of stages, not only for laboratory work but also for calibration and diagnosis on the field, with subsystems integrated in the own telescope. In this last case the compactness is not only needed to comply with size, weight and low cost requirements, but also to guarantee a high reliability and long lifetime.

The major applications for the development of miniaturised ns-range pulse generators in the CTA project are focused on the following fields:

Diagnostics of failures

A pulse generator able to reproduce the signals supplied by the PMT to the pixel chain is very helpful for fault diagnostics, since it makes possible a fast and convenient discrimination between Focal Plane Instrumentation (photodetector) and electronic failures. Achieving the necessary compactness to integrate it in the camera is a major challenge.

Photodetector testing and proof of concepts

CTA specific needs demand stringent requirements to the photodetectors in terms of quantum efficiency in the blue and UV range, as well as noise, bandwidth and reliability. A proper characterization of possible candidates to become camera photodetectors (as the PMTs or SiPMs) requires a number of different tests, namely:

a) Bandwidth and pulse shape integrity
b) Afterpulsing
c) Noise
d) Single photoelectron response

In all these tests it is necessary to illuminate the photodetector with ns pulses of blue/UV light. In principle, this can be accomplished by using commercially available pulse

generators, but the high cost of these units make them unsuitable in situations in which a number of different institutes are participating in high volume tests, as it occurs in CTA.

The electronics needed to perform the signal conditioning and digitizing of the photodetectors is implemented in a number of boards that must be tested not only to check the proper operation but also to assess the compliance with the requirements and specifications defined by the System Engineering Management of CTA.

Camera calibration

The nanosecond pulse generators presented in this thesis are also suitable for camera calibration. In order to calibrate the camera, the gain of each channel has to be accurately determined. The current system that is foreseen for the calibration of the LST cameras illuminates the camera with a light source of known intensity and measures the ratio between the single photo-electron and the number of digital counts recorded by the readout system. During the calibration, a light source produces a defined ns short pulse of UV light, triggered by software. The light beam is made uniform and widened in a way that the whole LST Camera including some margin for misalignment is illuminated.

Despite all the applications mentioned above, it is believed that the scope of the work here presented is not restricted to CTA, but can be applied in a wide variety of other fields. On the other hand the possibility of participating in the development of a large scale scientific facility as CTA opens many opportunities of gaining knowledge in high level system engineering procedures.

Organization of this thesis

Chapter 1 is started with a brief review of the basic principles of IACT telescopes, which are used in the detection of gamma rays. The interest in this field of research is due to the high amount of information that is possible to obtain, by means of the gamma ray study, about cosmic matter and the processes that take place in the universe.

Nowadays there are worldwide several projects based on this type of telescopes, among which the group where the author of this thesis belongs to has taken an active part in two of them: MAGIC and CTA. Chapter 1 continues with a summary of the most outstanding aspects of the MAGIC project, the starting point of this thesis.

Next, a detailed synthesis of the CTA project is carried out, which is the leading project in the Very High-Energy (VHE) gamma-ray observation field. Special attention is taken in aspects of design, goals, requirements and schedule.

There are three different sizes of telescopes, required for covering the entire energy range foreseen in the CTA project (between 20 GeV and 300 TeV). The summary is focused in the bigger one (LST, Large Size Telescope) in which the Spanish community is most involved, detailing each one of the parts that compose it. To conclude, the main requirements and benefits of the development of ns pulse generators for CTA are laid out.

In Chapter 2 a summary of different nanosecond pulse generator designs is presented. There are several topologies used in the design of Ultra Wide-Band (UWB) pulse generators, as for example those based on: 1) scintillators, whose emitted light is converted into electric signals by means of photomultipliers (PMTs), 2) transistor switching, with a wide range of different designs, 3) tunnel effect diodes, taking advantage of the special characteristic of this type of diode to achieve very fast transitions, and 4) non-linear transmission lines (NLTL), in which the non linearities cancel out the line dispersion, causing the narrowing of the input pulse.

Chapter 3 is focused on describing the most important figures of merit. Signal integrity, noise and jitter are essential parameters to be taken into account when designing UWB pulse generators. Knowing the main mechanisms that are likely to contribute to the generation of noise or distortion is essential when performing reliable and robust designs, as well as to do the right selection of the devices. A detailed analysis of the main elements that put at risk the integrity of the signal, and the main sources of noise and jitter, is shown in this Chapter.

Chapter 4 is focused on the design of a low jitter pulse generator based on a SRD (Step Recovery Diode), it is believed that this is one of the most successful contributions of this thesis. The design topology consists in a pulse sharpener, which is composed by the SRD, a short-circuited stub and a diode Schottky.

In particular, it has been developed a four channels prototype with output pulses of more than 4 V amplitude and widths in the order of the nanosecond, which has been used for testing the receiving boards of the MAGIC II telescope. Additionally, the generator design has served as a base for the manufacturing of a 96 channels board used in tests of the readout boards of the MAGIC upgrade and has been proposed for testing the readout system of the largest telescope of CTA.

Chapter 5 is devoted to the design of a new type of pulse generator (Signal On Transition pulser or SOT), which produces the pulses in the middle of the transitions of the control signal coming from a low bandwidth pulse generator. This device features several advantages as for example the immunity of the output pulse to ringing and distortion at the ends of the control signal transitions, or the possibility to modify the width of the pulses within the same PCB. In this SOT device it is possible to electronically tune the width of the pulses by modifying the slope of the control signal. A prototype with adjustable rise and fall transitions times is proposed.

Chapter 6 focuses on the validation and verification processes necessary for guarantee the compliance of the respective requirements and specifications established in CTA, with emphasis on those where the ns pulse generators developed in this thesis could be used. Especially outstanding are the requirements and specifications that make reference to the maximum illumination allowed and the issues associated to the overexposure, the specifications about the maximum latency times of the camera trigger system, or the specifications about the noise and bandwidth, especially limited by the PMTs.

Equally relevant are the specifications about the camera calibration, for which it is necessary a source of uniform light and variable intensity that emits light pulses under 2 ns to determine with accuracy the gain of the camera channels. Finally it is shown the importance of validating and verifying the reliability and robustness of the external amplifiers placed after the PMTs.

Following the traditional structure of a thesis, Chapter 7 shows a synopsis of the main achievements and conclusions obtained in the realization of this thesis, as well as several proposals of possible improvements and further researches are suggested.

Chapter 1. The CTA Project

1.1 Cherenkov radiation

Cherenkov radiation was discovered by P. Cherenkov in 1934 when he was investigating the effects of radioactivity in liquids, and shortly after explained by I. M. Frank and I. E. Tamm [1]. Frank used a simple model to study the composition of waves emitted by a moving source from each point in its path. He used the well known illustrative formulation of the Huygens principle in the form it appeared in his original book Treatise on Light, when he explained the reflection and refraction phenomena [2]. A deep historical perspective with interesting remarks and details of the first experiments has been published by B. M. Bolotovskii [3].

Figure 1.1 shows how the wave fronts of Cherenkov radiation are built. A charged particle moves from left to right with a speed v along the horizontal line that is higher than the phase velocity of the wave. Spherical waves emanate from the points the particle had passed. The propagation speed of these waves is equal to the phase speed of light c/n, where c is the speed of light in the vacuum and n is the refractive index of the medium. The surface of constant phase of the spherical waves emitted along the particle trajectory are cones with an apex at the particle position and an axis that coincides with the particle trajectory. In accordance with the Huygens principle, this conical surface is the front of the wave radiated in the motion of the charged particle. The propagation direction of this wave coincides with the normal to the conical surface, and the angle between the normal and the particle velocity is given by

$$cos\theta = \frac{c/n}{v} \tag{1.1}$$

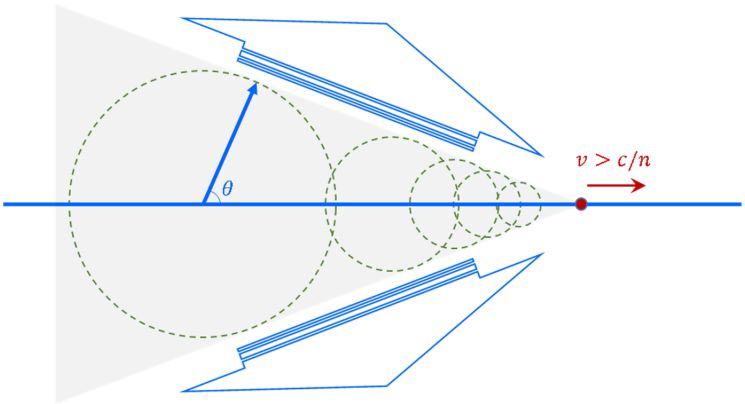

Figure 1.1 Cherenkov radiation cone created by a single charged particle.

When high-energy charged particles transit through optically transparent, refractive, dielectric materials, such as atmosphere, they interact with the atoms bonded to the molecules. As these particles interact with the atoms in the media, there are a number of mechanisms by which the energy may eventually be released including Bremsstrahlung, transition radiation, thermal motion, ionization, and Cherenkov radiation.

When a Very High Energy (VHE) gamma-ray comes into contact with atmosphere, it generates a cascade or shower of high energy secondary particles. The original gamma-ray produces an electron and a positron, and both of them lose a fraction of their energy by Bremsstrahlung creating a new, lower energy gamma-ray that starts again the process. The shower finishes when the gamma-rays do not have enough energy to produce new electron-positron pairs. Many of the resulting charged particles move at very high speeds. When they exceed the speed of the light in the atmosphere, they emit Cherenkov radiation.

Figure 1.2 illustrates how a gamma-ray coming from a source gives rise to a cascade of particles generating Cherenkov radiation. The Cherenkov photons cover a broad frequency range, being the higher frequencies (UV) the most common ones. As a result the Cherenkov light appears to be a bluish white, although it actually has a broad spectrum where the UV frequencies are the dominant ones.

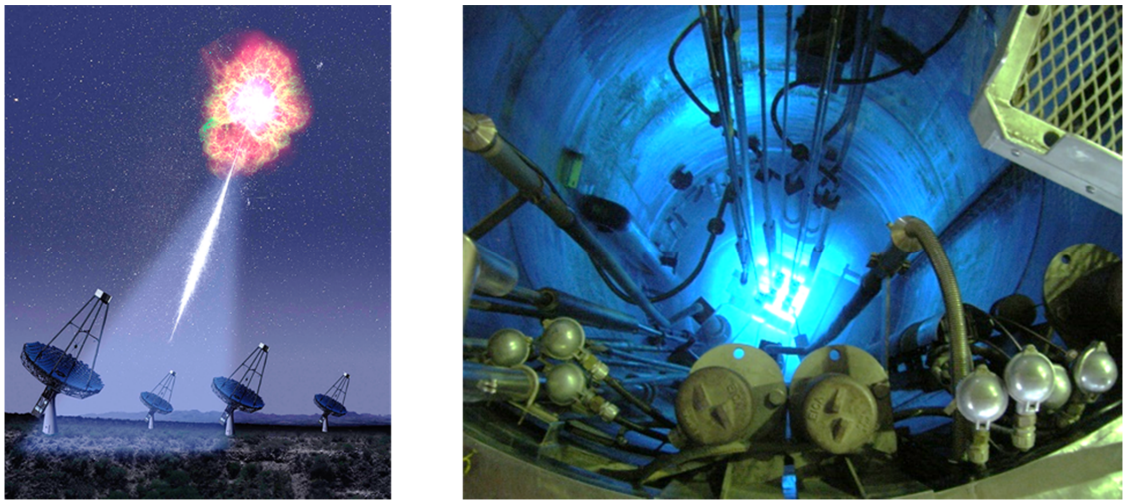

Figure 1.2 Artistic view of a gamma-ray entering into the atmosphere (left) and Cherenkov radiation observed in the R-6 reactor of the Bariloche Atomic Center in Argentina (right).

Most of the shower maximum development happens at an altitude above sea level from 20 to below 10 km, value that depends on the initial particle energy. The altitude for optimum observation decreases as the particle energy increases. Imaging atmospheric Cherenkov telescopes (IACTs) detect this light and reconstructs the shower. Reconstructing the shower axis in space and tracing it back onto the sky allows determining the celestial origin of the gamma-ray. Moreover, the intensity of the image is related to the energy of the gamma ray. It's important to underline that the origin of gamma rays is possible to be known because, as they do not have electric charge, they do not interact with anything along its

travel from the source to the Earth. In particular, these rays are not affected by the magnetic fields surrounding the Earth.

The Cherenkov light intensity per unit area is low and its time interval arrival is short, of about a few nanoseconds. For these reasons, extremely sensitive and fast detectors are required. Optical reflectors size must be maximized to collect enough light and the camera elements (photomultiplier tubes) must detect individual photons with high efficiency. The effective area of the detector is about the size of the Cherenkov pool at ground. That is, for example, about 50,000 m^2 for an air shower initiated by a 1 TeV gamma ray. Also, the telescope will be used in dark nights at clear sites for avoiding background light.

Cosmic rays, more common than gamma rays, undergo a similar process when they arrive to the atmosphere, creating air showers as well. Gamma rays are photons, whereas cosmic rays are high energy charged particles consisting mainly of protons and atomic nuclei (98%) and electrons (about 2%). They generate background noise that masks the measurements of a gamma ray detector. However, the image they produce in the detector is different from that created by gamma rays, and then can be discriminated.

1.2 The MAGIC telescopes

Very high-energy (VHE) electromagnetic radiation reaches Earth from a large part of the Universe, carrying crucial and unique information about the most energetic phenomena in the Universe. Yet, only for the last 25 years have we had instruments that can “see” this radiation [4]. Over that time, Imaging Air Cherenkov telescopes (IACTs) and air shower detectors have developed very rapidly, and opened up a new window for the exploration of the Universe. Figure 1.3 shows the current IACT instruments, MAGIC [5], H.E.S.S. [6] and VERITAS [7] telescope systems, together with the Fermi satellite [8]. They have produced a number of high impact results and demonstrated the importance of observing VHE phenomena. The first steps of this thesis were taken during the participation of the author in the MAGIC project.

The MAGIC telescopes are two Imaging Atmospheric Cherenkov Telescopes (IACTs) located on the Canary island of La Palma. The telescopes are designed to measure Cherenkov light from air showers initiated by gamma rays in the energy regime from around 50 GeV to more than 50 TeV. They started to operate in 2004 and 2009, respectively, with different cameras, triggers and readout systems. In the years 2011-2012 the MAGIC collaboration undertook a major upgrade to make the stereoscopic system uniform, improving its overall performance and facilitating its maintenance [9]. In particular, the camera, receivers and trigger of the first telescope were all replaced and the readout and calibration box of both telescopes was upgraded.

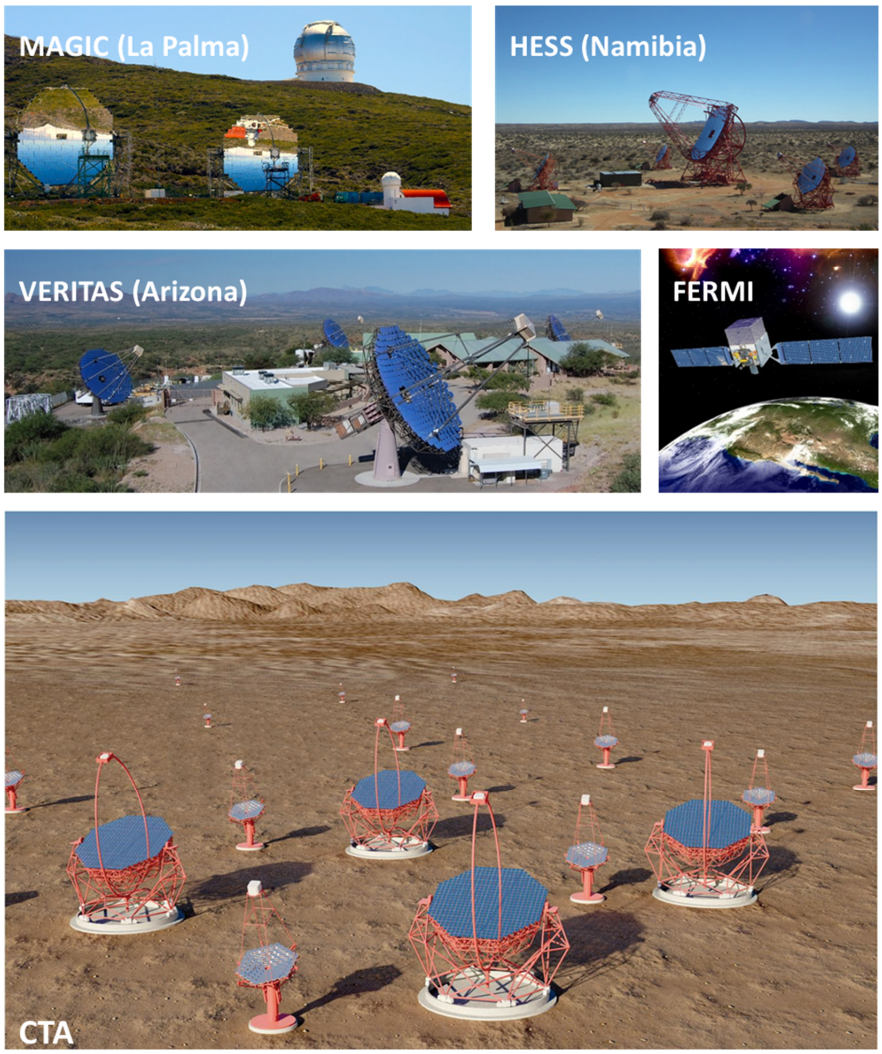

Figure 1.3 Current installations involved in VHE research and artistic impression of the CTA-South observatory.

The first MAGIC I camera was composed of 577 high speed, high quantum efficiency photomultipliers. The new one has 1039 channels and follows closely the design and performance of the MAGIC-II camera. The photosensors are photomultiplier tubes (PMTs) of one inch diameter, with a hemispherical photocathode and 6 dynodes. Each pixel module includes a compact power unit providing the bias voltages for the PMT and a stack of round circuit boards for the front-end analog signal processing. A mathematical estimation of the photodetector response to the light generated by a source can be found in Appendix A.

The data in MAGIC telescopes is transmitted via optical fiber to the Flash-ADC located in the control house. The digitization is performed by a state of the art DAQ system consisting of a dedicated chip called `Domino Ring Sampler`. The analog waveform is stored by means of a capacitor array and next it is read out and converted via a commercial ADC. The whole structure is able to point to any place in the sky in less than 40 seconds, which makes it the fastest existing Cherenkov Telescope. An important contribution to the

electronics of the MAGIC II telescope was carried out by Pedro Antoranz (member of the UCM-ELEC) in his doctoral thesis [10], whose last period was overlapped with the beginning of the work here presented.

The need for compact pulse generators able to provide clean pulses in the ns range emerged soon within the MAGIC collaboration. The analog part of the MAGIC telescope acquisition chain must process Cherenkov light pulses with widths ranging between one and ten nanoseconds, and amplitudes ranging from tens of microvolts to five volts for a fifty Ohm load. The camera pixel signals are converted to optical signals via Vertical Cavity Surface Emitting Lasers (VCSELs), and transmitted via optical fibers with lengths of more than 162 m to the control room where an array of receiver boards perform the analog to digital conversion and signal processing. The development of an evaluation board based on a Step Recovery Diode (SRD) pulser was one of the main contributions of the author of this thesis to the MAGIC experiment [11]. The prototype was not only used for the tests of the MAGIC II receiver boards, but also inspired further designs for the validation of the RAMS requirements in CTA, which are also described in this thesis.

1.3 CTA Concept, Goals and Schedule

The Cherenkov Telescope Array (CTA) is the leading project among all current designs of future Very High-Energy (VHE) gamma-ray observatories. It is ranked as one of the top priorities by the European Astroparticle roadmap (ASPERA) and the European Astrophysics Roadmap (Astronet). It has also been included in the roadmap of large scientific facilities in Europe (ESFRI) and as a High Priority Project in the Spanish Strategy for the participation in Scientific Infrastructures in 2010.

The Cherenkov Telescope Array (CTA) is an observatory for very-high-energy gamma-ray astronomy, which will provide observers with data on astrophysical objects over a very wide range of energies with excellent sensitivity, between 20 GeV and 300 TeV. The CTA Observatory – operating arrays of Cherenkov telescopes on two sites, one in each hemisphere – is intended to provide a service to a wide scientific community, beyond those institutes currently involved in the design of the instrument and in the preparation of its construction.

The CTA project was initiated and is currently being developed by a group of institutes known as the CTA Consortium. The CTA Consortium formed in 2008 and is organised by a Memorandum of Understanding (MoU). Supported by the EC Preparatory Phase grant (CTA-PP, Grant Agreement N° 262053) [12] and the national funding agencies of the participating countries, the Consortium comprises over 170 institutes in 28 countries, with over 1000 members, as shown in Figure 1.4. Spain participates with 9 groups. The author of this thesis is affiliated to one of them, UCM-ELEC. In 2013 CTA entered the Pre-Construction Phase (CTA-

PCP), which overlapped until summer 2014 with the CTA-PP. On basis of an evaluation by an ESFRI expert group, CTA was found eligible for support under H2020 – INFRADEV 2015-3.

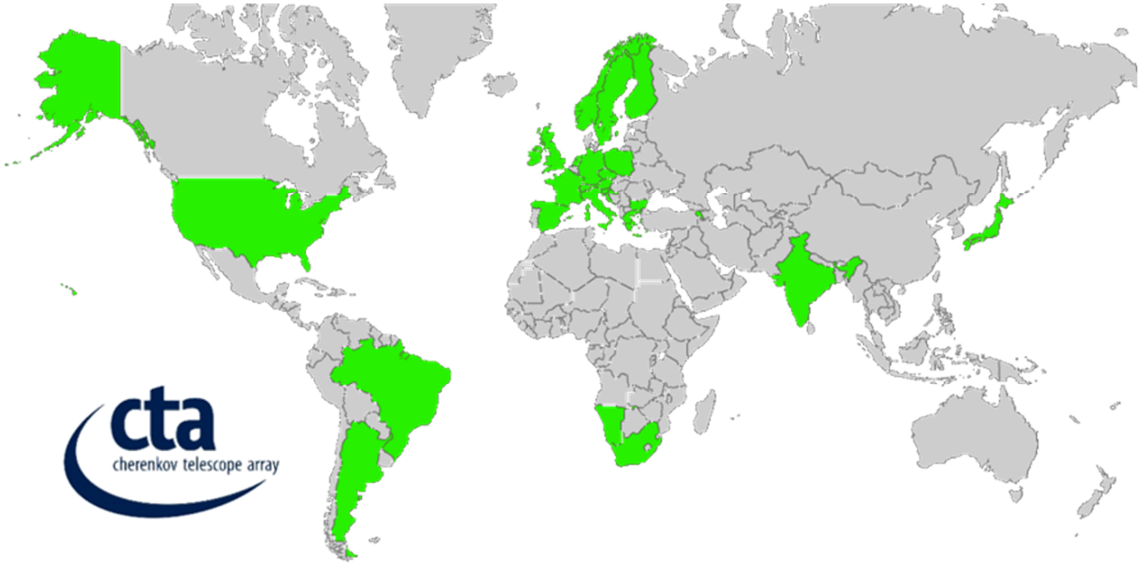

Figure 1.4 Countries with institutions participating in CTA Project.

At the time of writing this thesis, a funding and construction agreement among the participating countries is pending to be reached, and then the CTA Construction Phase (CTA-CP) will start. By this time it is expected to close the design of all the telescopes and auxiliary instrumentation, as well as to qualify the production technologies, an effort that is expected to take benefit of some of the results of this thesis.

CTA builds on the proven technique of detecting gamma-ray induced particle cascades in the atmosphere through their Cherenkov radiation, simultaneously imaging each cascade stereoscopically with multiple telescopes, and reconstructing the properties of the primary gamma ray from those images. Through deployment of a large number of Cherenkov telescopes per site at two sites in the southern and the northern hemispheres, CTA will achieve full-sky coverage. By the time of writing this thesis, the sites were recently chosen after a long selection process. El Roque Observatory, at La Palma island (Spain), has been elected as the northern site whereas the Paranal Observatory, at Atacama desert (Chile), has been chosen as the southern site.

More than a thousand of new source detections are foreseen over the lifetime of the array [13]. But besides the interest of discovering new VHE sources in the Universe, a number of Science issues can be addressed with CTA. The observatories can provide valuable information to study the mechanisms of cosmic particle acceleration [14]-[16] and demonstrate the potential of accelerated particles in the study of star formation and galaxy evolution [17]. It also can help to investigate extreme environments like neutron stars and black holes, as well as active galactic nuclei [18], [19] and compact galactic sources in the

GeV–TeV γ-ray energy range [20]. A number of researchers expect to take benefit of CTA in their studies on Dark Matter [21], [22], the Universe opacity [23], gamma-ray bursts [24], [25], pulsars [26] and binaries [27]. Others aim to use CTA to give answers to fundamental questions of Physics, like the violation of Lorenz invariance [28]. CTA has also a potential to do optical intensity interferometry [29].

Technical developments in the context of CTA, such as the development of improved photomultipliers, high reliability electronics or high-volume production techniques for mirror facets are starting to find applications in other fields. The references [30] and [31] describe in detail the major technical contributions. An impression of the increase in activity and interest of CTA may be gauged by the number of papers presented at conferences by CTA members as registered with CTA's Speakers and Publications Office. This is shown in Figure 1.5. At the time of writing this thesis there were 124 CTA contributions to conferences in 2014 registered. Many of the conference contributions have been invited talks, a good indication of the wider impact of CTA.

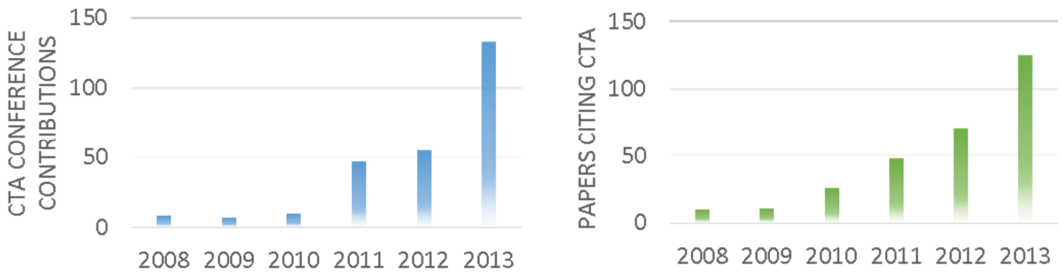

Figure 1.5 Conference contributions from CTA Consortium members (left) and published papers mentioning CTA, according to the NASA Astrophysics Data System (right).

Another dissemination route to the scientific community is via journal publications. A highlight has been the publication of the special edition of Astroparticle Physics in March 2013, containing 346 pages of papers about CTA and its scientific impact written by members of the CTA Consortium and experts from outside the Consortium. Despite being published for only just over a year, these papers have received 180 citations. To date, according to the NASA Astrophysics Data System there have been over 300 publications which explicitly mention CTA and its scientific properties. Figure 1.5 also shows how the number of these papers has increased during the Preparatory Phase. Many of them were written by scientists who are not members of the CTA Consortium, but who have been attracted by the scientific possibilities offered by CTA.

CTA contains instruments with small-, medium-, and large-sized reflector dishes with different designs in order to cover a broad energy range of observations. The position of each telescope was optimized with the aid of Monte Carlo simulations, which helped to find the best cost effective solution for the target scientific goals and also provided the first estimations of CTA sensitivity [32]. The project is currently entering in its Preconstruction Phase, whose goal is to finish the design of all of its parts and validate all the prototypes.

Throughout 2015 the construction of full, operational prototypes of each telescope type is being carried out. Regarding the prototype of the Large-Size Telescope (LST), in which the Spanish community is most involved, will be installed along 2016 in the Roque de los Muchachos observatory, in the Canary island of La Palma. Eight LSTs (four at the Northern Hemisphere and four at the Southern one) will be built.

As a prerequisite for the final design, CTA requirements were established on the basis of science goals and technical feasibility. The requirements were developed with the intention of defining precisely what CTA should be able to do. They are defined and documented at four levels, as shown in Table 1.1.

Level A requirements concern the CTA Observatory as a whole. The Level B requirements define key telescope parameters, requirements on the optical and mechanical systems, camera requirements and requirements regarding synchronization, trigger, and data readout as well as Observatory operation and Observatory infrastructure. To the extent possible, requirements were defined in an implementation-independent fashion. Requirements at lower levels flow down from higher-level requirements, and are managed via a database. Level C lists product specifications defined by the product teams on the basis of the requirements.

General requirements	The CTA Observatory CTA Basic Definitions Science Requirements
Level A CTA requirements	Performance Requirements Reliability, Availability, Maintainability and Safety (RAMS) Requirements Environmental Requirements End-User Requirements
Level B CTA requirements	Observatory Operations Requirements Infrastructure Requirements Data Management Requirements Array Control Requirements LST Requirements MST Requirements SCT Requirements SST Requirements
Level C Specifications	Observatory Operations Specifications Infrastructure Specifications Data Management Specifications Array Control Specifications LST Specifications MST Specifications SCT Specifications SST Specifications

Table 1.1 CTA requirement and specification categories.

The CTA group to which the author of this thesis is affiliated first focused its work on the Reliability, Availability, Maintainability and Safety (RAMS) plan development for the entire CTA observatories [33]-[35] and the corresponding RAMS requirements [36]. Once the top level organization was defined, the group joined the LST project to develop the RAMS work on the LSTs and in particular the validation of the RAMS requirements for the LST [37]. The development of compact ns-range pulse generators is part of these efforts [38]-[40].

1.4 The Large Scale Telescopes (LST) of CTA

This section and the forthcoming one are a brief summary of the LST Technical Design Report [41] and are added here to better understand the framework in which this thesis was developed. Figure 1.6 shows a simplified sketch of the LST structure and the top level of the Product Breakdown Structure. The LST structure is based on the MAGIC one. By the time of writing this thesis the design of the telescope is almost closed [41]. The interface control documents are being developed and decisions were taken to build the first LST in The observatory "El Roque de los Muchachos" at La Palma, were a major test campaign is foreseen to definitely proof the concept under real world conditions and to demonstrate compliance with several requirements and specifications that cannot be validated by either software or laboratory tests.

The main elements of the telescope are:

- Mechanical System: contains the mechanical structures and the civil constructions.
- Optical System: includes the reflective surface and the electro-mechanical system, so called AMC, which makes the optics active.
- Camera: is a close case that incorporates the photo-sensors, the front end electronics and the readout system.
- Auxiliary Systems, with all the remaining items that are not mentioned in the previous assemblies, as for instance the Energy Storage, the pointing system, the calibration system, etc.

The LST is an alt-azimuth telescope. The telescope has a 23 m diameter reflector composed of 198 hexagonal mirror tiles of ≈2 m^2 area each. The reflector has a gross parabolic profile in order to minimize additional time spread of the very fast Cherenkov light flash, and is supported by a tubular structure made of CFRP, steel and aluminum tubes. With a total surface of 400 m^2, it collects and focuses the Cherenkov radiation into the camera, where 1855 photo-sensors convert the light in electrical signals that can be processed by dedicated electronics. The total weight of the telescope is around 100 tons.

The camera has a field of view of about 4.5^o and has been designed for maximum compactness and lowest weight, cost and power consumption. Each pixel incorporates a

photo-sensor and the corresponding readout electronics. These electronics are based on the DRS (Domino Ring Sampler) chip, which is currently used in the MAGIC experiment.

The camera trigger strategy is based on the shower topology and the temporal evolution of the Cherenkov signal produced in the camera. The analogue signals from the photo-sensors are conditioned and processed by dedicated algorithms that look for extremely short but compact light flashes. Furthermore, the LSTs cameras are interconnected in order to form an on-line coincidence trigger among the telescopes, which allows to efficiently suppress accidental triggers.

Guaranteeing full compatibility among the camera modules of the telescopes is challenging. For the MST camera two possible designs are presently under study: NECTAR cam and flash cam. NECTAR cam modules have been designed to be interchangeable with the LST cam ones. Extensive work has been undertaken to figure out common interfaces and common components. This allows to optimize the resources, lower the capital investment cost and facilitate the maintenance of the observatories.

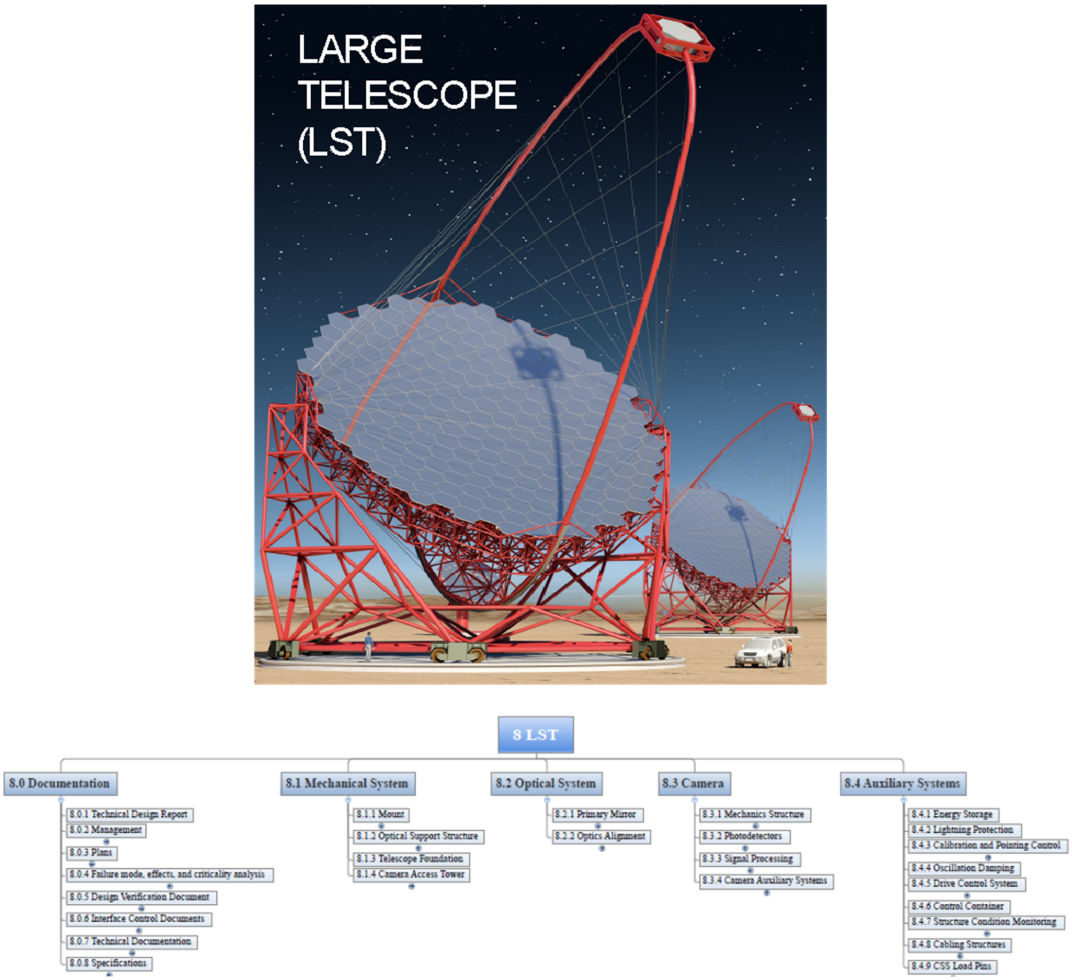

Figure 1.6 Artistic impression of CTA large scale telescope and top level product breakdown structure.

A high rate of photons from the night sky background fluctuations makes an efficient detection of the Cherenkov light, produced by the gamma-ray showers, a very challenging task. In fact, the NSB (Night Sky Background) enters into the photo-sensors of the Camera focal plane with a rate of the order of 100 MHz. Typically, the Cherenkov photons simultaneously hit neighbor photo-sensors, forming compact images at the focal plane of the telescope. On the other hand, the light due to the NSB follows a Poissonian distribution and rarely forms compact images. Therefore, the single telescope trigger requires a given number of close photo-sensors with a minimum number of photons and in a narrow time window of few nanoseconds. Moreover, the rejection power of the NSB becomes more effective, if the constraint to record the same event in two or more telescopes is introduced. A further key goal of the LSTs is its ability to reposition to any point of the sky in less than 20 seconds. This makes it instrumental in the study of fast transient phenomena and in particular Gamma Ray Bursts.

The mirror tiles are supported by a large space frame made from high strength carbon fiber (CF) reinforced tubes. In order to correct small deformations of the mirror due to sagging of the support frame, each mirror tile is corrected by the so-called active mirror control (AMC). The mirror dish is mounted onto the telescope substructure made also from large diameter high strength steel tubes linked to six bogies running on a circular rail. The substructure is also connected to a central axis fixed anchored in the concrete foundation.

The telescope uses a concrete foundation weighing about 400 tons. In order to prevent telescope lift-offs during strong storms the bogies are secured around the rail, which in turn is also fixed to the concrete foundation. The telescope is driven by azimuth and elevation servomotors. An access tower allows one to access the camera when the telescope is in its park position during day-time. It also serves as an anchor for the telescope camera to secure the telescope during strong storms.

The camera will be supported by a single arch camera support mast construction, similar to the construction of the MAGIC telescope design. The parabolic shaped mast will be made from a curved tubular CF construction of 34 cm Ø. Transverse stability will be enforced by a number of high strength, low expansion, pre-stressed CF-cables (used for sail boats or in oil industry). The construction resembles a deformed bicycle wheel-like configuration. The f/D is 1.2, i.e. the camera is located 28 m above the mirror (reference mirror center).

The current design of the CTA Observatory includes eight LSTs, four in the CTA-North site and four more in CTA-South. The LST working package has planned the manufacturing of the telescopes with the goal of producing all the telescopes over six years, from the beginning of the installation of the first LST by the end of 2016 to the end of commissioning of last telescope in 2021. The LST development differs from other CTA telescopes as the first LST is being manufactured as a prototype, but a fully functional one that eventually becomes the first LST of CTA (Pre-Construction), once commissioning finishes and is verified it fulfils all CTA requirements. This decision is motivated by the relatively small number of units to be produced and the elevated cost of each individual telescope. The first telescope will be

retrofitted if it is found that design modifications are needed during commissioning, to ensure equal performance to the rest of LSTs. The second telescope will mark the beginning of the LST (Construction phase). Several elements manufactured in workshops of participating institutes will be subcontracted to industrial partners. Orders will be timed based on the experience obtained during the construction of the first LST, aiming for a peak construction rate of two telescopes per year.

The current best estimate for the cost of the first LST is around 9.5 million Eur, excluding taxes, spares, contingency and labor in the institutes. In the production phase, the cost per telescope is estimated to be around 8.4 million Eur, assuming a production of seven telescopes in the planned interval and that the same PMTs are used in MST and LST Cameras.

The LST project team consists of more than 100 scientists from eight countries: Brazil, France, Germany, India, Italy, Japan, Spain and Sweden. Representatives from countries with the largest contributions to the LST (currently France, Germany, Italy, Japan and Spain) form the Steering Committee, where the allocation of the resources and manpower for the LST project is discussed. The development, production and evaluation of the LST elements is supervised by the Executive Board, which consists of Principal Investigator and Co-Principal Investigator, Project Managers, QA/RAMS Manager, System Engineer, and the coordinators of individual sub-assemblies.

1.5 The camera of the LST (LST-CAM)

The camera of the first prototype comprises 1855 pixels of 0.1° diameter. Each pixel consists of a light collector of hexagonal input pupil and a 1.5 inch spherical window photomultiplier of only 8 dynodes of around 10^4 gain, followed by an AC coupled fast preamplifier and the digitizer and readout electronics. Parallel trigger electronics will generate triggers. Nearly all the electronics will be installed in the camera with a maximum weight of 2 tons.

The LST-CAM is based on a modular design with all the electronics on-board. It is conceptually divided in three main parts:

- The Focal Plane Instrumentation (FPI),
- 265 modules of seven pixels that contains the front-end electronics, and
- The global and auxiliary camera elements.

These three parts are also physically separated inside the camera. Looking from the entrance window, where the light collected and reflected by the mirror surface enters, one sequentially finds the FPI, the module and finally the global camera elements. The camera architecture is presented in Figure 1.7. All the optical and electronic devices need mechanical structures, which serve both as skeleton and skin. The former part sustains all the elements

of the camera, the latter provides protection from the external environmental conditions and the interfaces to whatever is physically outside the camera. Finally, in the external part of the mechanical structure, some auxiliary elements are placed.

The FPI includes the following important subsystems:

- Entrance Window
- Light Concentrators
- Light Sensors (the PMTs)
- HV Power Supply
- Pre-amplifier
- Slow Control board (SCB) and Pulse Injection

The pulse injection system essentially consists of a compact ns-range pulse generator which is integrated in the FPI for diagnostic purposes. It aims to reproduce the signal supplied by the photomultiplier to the analog readout electronics when the sensor is excited by Cherenkov radiation. The performance requirements for this device are very demanding in terms of cost, reliability and light weight. The camera weight is a particularly critical parameter, since the telescope must be repositioned at very high speeds when a gamma ray burst alert is issued.

The pulse injection subsystem is inspired in the one developed for MAGIC telescopes. The current PMT pulse width at nominal HV for the first LST of CTA is in average around 2-3 ns FWHM [42]. Some of the pulse generators proposed in this thesis are even capable of providing shorter pulses, which makes them also valid for future and innovative faster photo-sensors. The pulse injection is demonstrating to be a very valuable diagnostics tool in MAGIC allowing for daily tests of the whole chain, from the PMT base down to the readout and trigger, without applying a high voltage to the PMTs.

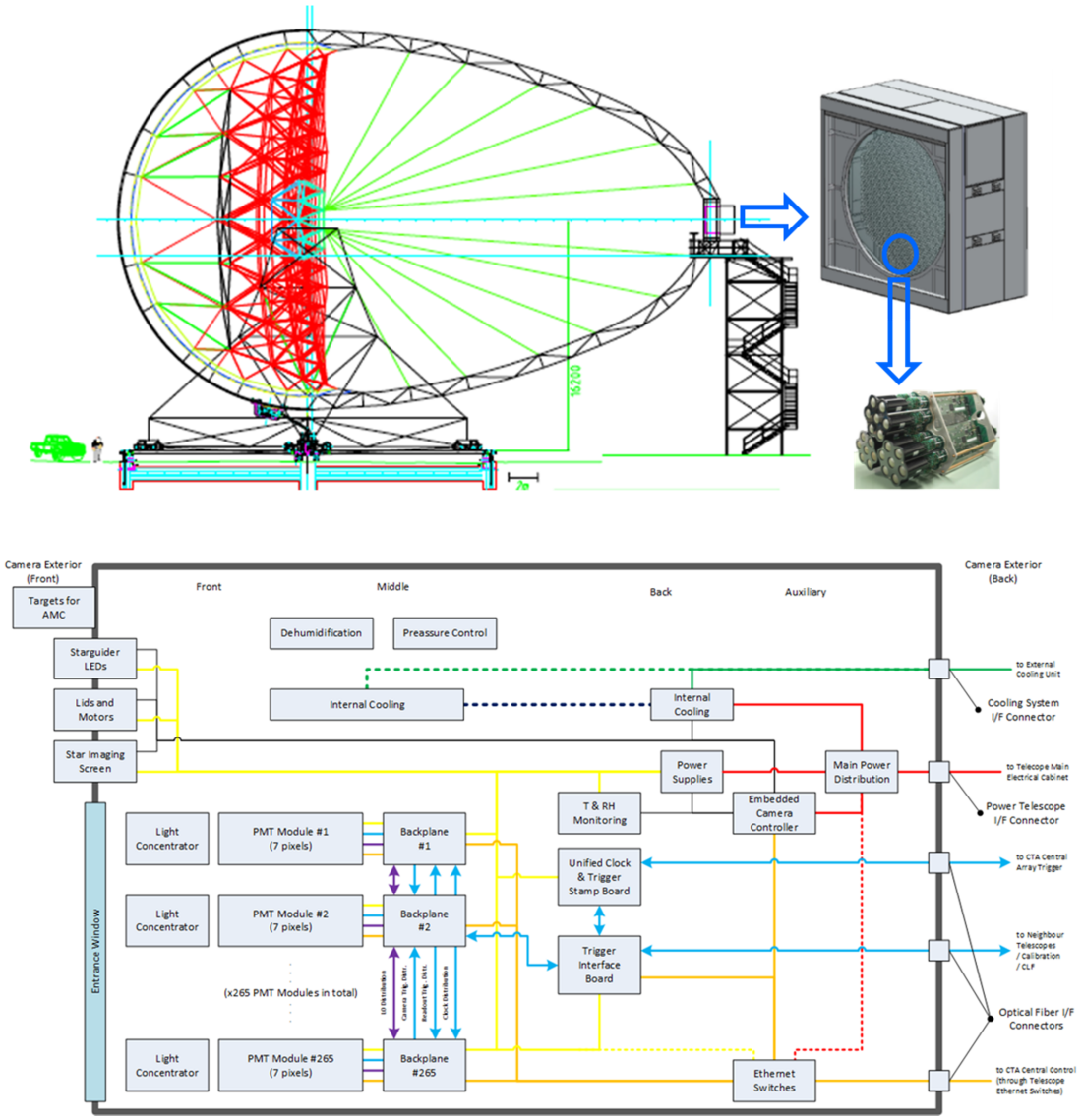

Figure 1.7 Details of the LST camera structure.

Every 7 PMTs module hosts a readout board creating a modular system which follows the cluster layout. This board, developed by the Japanese groups of LST, is shown in Figure 1.8. The green arrows mark the path of the analogue signal from the PMT, which undergoes a pre-amplification, it crosses the SCB and finally enters into the readout board. In the pre-amplification by PACTA, the PMT signal is split with two different gains to increase the dynamic range, and then digitalized in the Readout Board. Another signal is generated in the Readout Board from the PACTA high-gain output to be used as a selection command to digitalize only the events of interest, reducing as much as possible the dead-time. On the right, the readout board is connected to a backplane that implements several I/O functions (blue and violet arrows), as for instance the intercommunication among the Modules for the trigger logic, the clock distribution and trigger array. The black arrows are simple control

lines, the yellow ones represent the low voltage power distribution, whereas the red ones the high voltage.

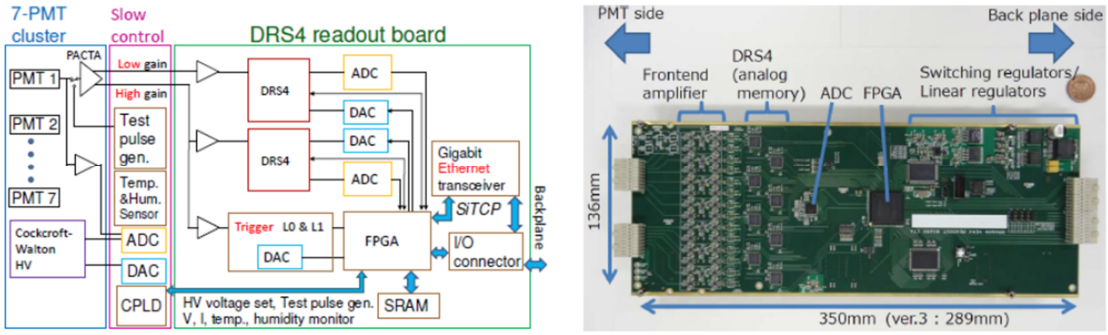

Figure 1.8 Readout board for the LST-CAM modules.

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Chapter 2. Nanosecond pulse generators

2.1 Pulsers based on scintillators

A scintillator is made of a luminescence material, which emits a small amount of light by fluorescence or phosphorescence when it is crossed by a charged particle or a gamma photon which ionizes the material. The emitted light can be either used as a test signal for phodetector diagnosis or converted to an electronic pulse with a photomultiplier tube (PMT). This was one of the most popular pulse generation techniques for particle physics research during the eighties and nineties [1].

The shape and duration of the scintillator signal gives additional information about the nature of the particles crossing it and, for this reason, the system scintillator - PMT became a well-known procedure to detect radioactivity in nuclear and particle physic installations. Firstly, the intensity of the emitted light is directly proportional to the energy of the ionizing particle going through. Secondly, the scintillator is very fast and therefore one can study with high accuracy the frequency of the phenomena. Finally, when analyzing the pulse shape at the PMT output, one can determine the particle type which goes through the scintillator detector.

In a previous work of the group, a plastic scintillator was used to design a pulse generator for the testing of MAGIC I pixels [2]. Figure 2.1 shows a schematic of the device. The emitted light is guided to the PMT, which is coupled to the scintillator by a light guide.

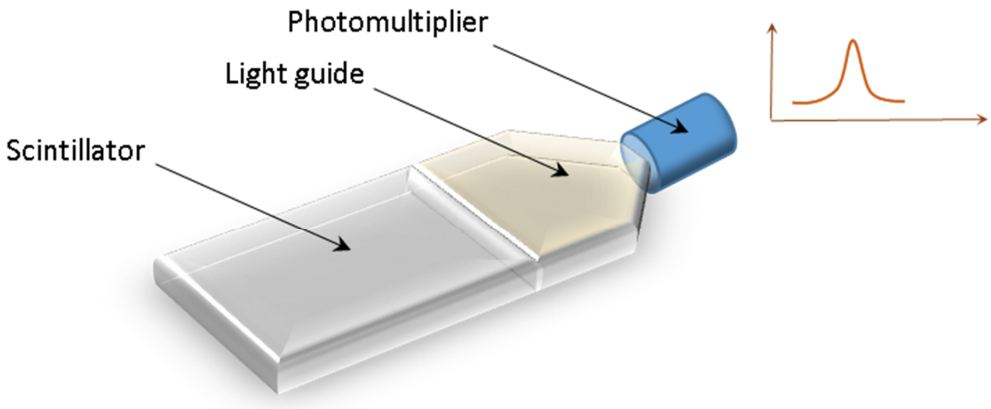

Figure 2.1 Pulse generation based on plastic scintillator.

This device produces pulses of short duration, since the re-emission time of the light impinging on the material is of the order of nanoseconds. A sample of Thorium of low radioactivity placed on the scintillator was used to excite the material. The device was able to naturally resemble the random nature of the arrival times of Cherenkov photons under real world operation, but limitations soon became evident since the generator was bulky and did not allow to control basic test parameters like the pulse repetition frequency, amplitude or width. On the other hand signal integrity and mismatch issues emerged from the PMT impedance.

2.2 Transistor based generators

There are a number of nanosecond pulse generator designs based on transistor topologies. Conventional, discrete, silicon transistors have been widely used to perform switching and amplifier functions. In order to generate fixed rise time pulses, RF transistors are biased in a switching (ON/OFF) mode. To avoid the saturation region is a critical issue since that would slow recovery time and consequently limit the maximum repetition frequency. For such purpose the circuit arrangement shown in Figure 2.2a can be used, where an emitter-coupled differential pair is connected to the output stage of the pulse generator [3]. In this design the emitters of transistors Q1 and Q2 are supplied by a constant current source and they are not allowed to enter into saturation, switching just between the linear region and off state. Outputs with both polarities are available. The output impedance of the circuit is set by the resistors Rg1 and Rg2 (typically 50 Ω). Pulses of 2 V amplitude (into 50 Ω) and 1.5 ns rise/fall times can easily be achieved with conventional, discrete, Si RF power transistors.

Adjustable rise time pulses are possible. Linear rising and falling edges can be produced by charging and discharging a capacitor with constant current sources, as shown Figure 2.2b. Decade changes in rise/fall time are set by just selecting several timing capacitors. Fine tuning is performed by adjusting the constant current sources.

The voltage across the capacitor C is amplified/buffered by the linear transistor amplifier. The output PNP and NPN transistors (Q1 and Q2) are operated as high output impedance, constant current sources. A shunt resistor sets the output impedance: Rhi (1 kΩ) or Rg (50 Ω). Adjustable pulse rise and fall times as fast as 2.5 ns, at maximum repetition rates of 150 MHz, and pulse amplitudes up to 10 V into 50 Ω can be achieved with this design. Furthermore, higher voltages are possible if the resistor Rg is switched out. Variable repetition rates, delays, durations as well as rise/fall control can be implemented with conventional TTL or ECL logic ICs.

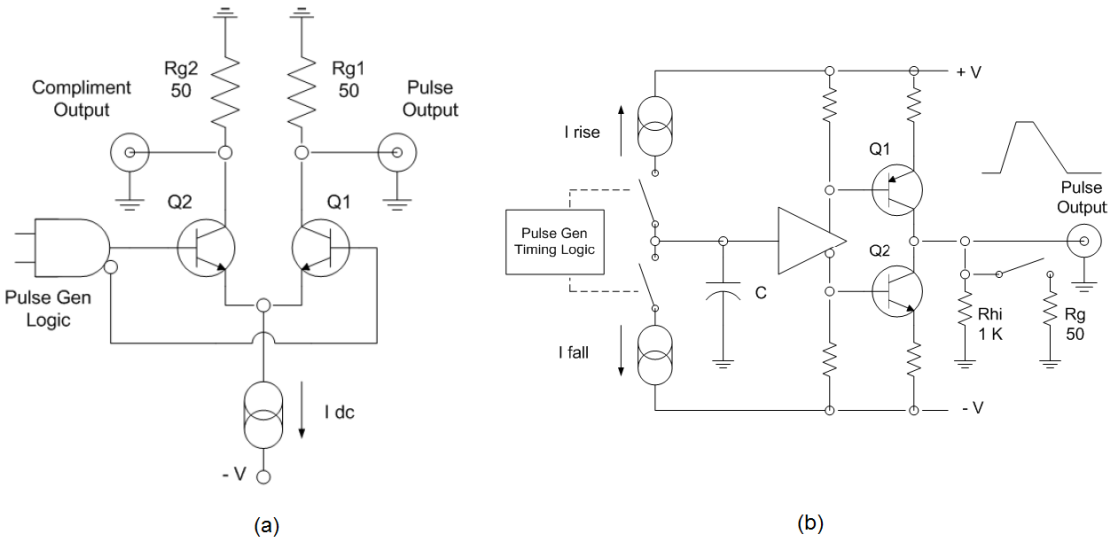

Figure 2.2 Transistor based pulse generators

Figure 2.3a shows the schematics of another pulse generator based on the Schmitt Trigger inverter. The basis of this generator lies in the hysteresis behavior of this device. The generation of pulses with tunable frequency and duty cycle is achieved by means of the asymmetry in the feedback network.

In this design the state of the inverter is controlled by means of the charge of the capacitor connected at its input. When it is discharged, the output of the inverter is at high level. Consequently the current flows towards the capacitor through resistor R1 with a time constant of R1·C1. When the voltage across the capacitor reaches the positive threshold voltage of the inverter, this one switches to low state. The capacitor discharges then through both R1 and R2 with a time constant of (R1//R2)·C1. Adjusting the values of the resistances makes possible to control the repetition frequency and the pulse width.

Another option of pulse generator based on digital logic is shown in Figure 2.3b, which is the solution adopted in the MAGIC pulse injection system. The 74AC14 block produces a square signal that feeds the next stage of the design. This time the asymmetric feedback network of the previous design is replaced by a single resistor, thus obtaining similar paths for the charge and discharge of the capacitor. The square wave is then fed into a second inverter, and both signals into an AND gate.

The 'AND' function of the square wave and its inverted would be a logical zero, but as there exists a delay in the propagation of the signal through the gates, a pulse is produced at the output of the AND gate. The amplitude of the pulse is ideally the bias voltage of the gate and its width is equal to the delay of the inverter gate (typically 2-4 ns). Nevertheless, the rise and fall times of the inverter make the actual pulse width to be slightly smaller than the bias voltage.

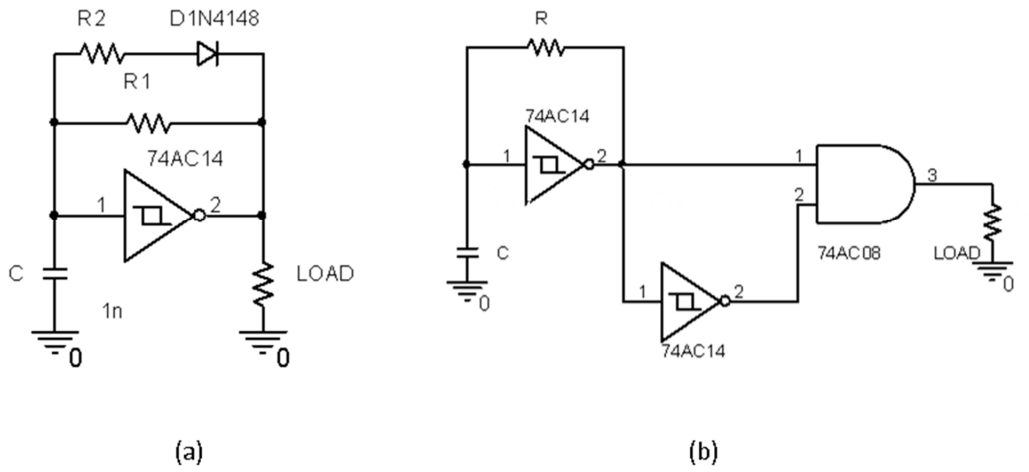

Figure 2.3 Asymmetric pulse generator (a) and pulse generator based on an AND gate (b).

2.3 Tunnel diode-based pulse generators

Figure 2.4 shows an example of a pulse generator based on a tunnel diode (TD), proposed by Andrews in [3]. A very stable low voltage, bias source is needed to bias the TD to point A on the I-V curve. Point A is set around 1% below the peak current. For AC purposes, this bias voltage is isolated from the TD by a large inductor, L1. A positive triggering pulse is coupled to the TD via capacitor C and a small inductor, L2. The extra triggering current causes the TD current to exceed the maximum one and pushes the operating point to B, which is in the negative resistance region and is unstable. Thus, instead of remaining at B, because the diode is being fed with a constant current (due to L1), the TD's operating point rapidly switches to the stable operating point C. In doing so, the voltage across the diode suddenly experiences a sizeable jump. The "tunneling" phenomenon inside the TD junction is essentially instantaneous. The terminal voltage transient conditions are determined by the diode's junction capacitance C_{TD} and its peak current rating, I_{peak}. The diode's switching time can be estimated closely by the simple equation:

$$\tau_{TD} = C_{TD}\frac{V(C) - V(A)}{I_{peak}} \tag{2.1}$$

During this switching time the nH range inductor L2 (much smaller than L1) forces all of the voltage pulse energy to travel towards the right to the pulse generator output. The TD's effective impedance is quite low when it is at point C. Thus, a series resistor, Rg, is used to set the output impedance of the generator to 50 Ohm. The output voltage into the external 50 load is about V/2. With a large H inductor used for L1, it will continue to push a constant

current of I_{peak} through the TD for a few seconds, thus creating a long flat-top, step-like pulse. Eventually, however, L1 cannot maintain this current indefinitely, and the operating point shiftes to point D. When it reaches this point, the device again enters its unstable region and rapidly switches to the new stable operating point E. From E the current through L1 slowly increases until the diode once again reaches its stable, initial operating point A set by the dc bias voltage source. If point A were to be biased into the negative resistance region, this circuit would operate as an oscillator rather than a triggered pulser. The oscillation period, or the pulser recovery time, is determined by the size of the inductors L1 and L2.

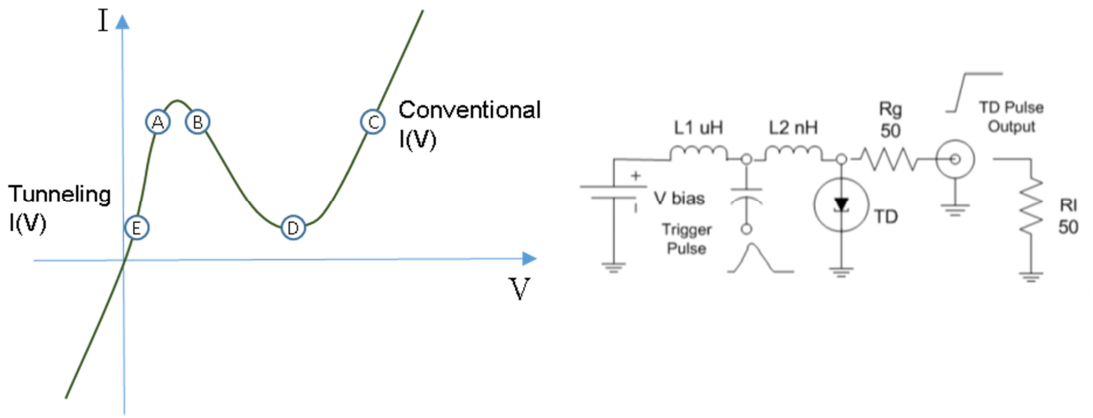

Figure 2.4 IV curve of a tunnel diode (left) and TD pulse generator (right).

2.4 Non linear transmission line pulse generators

The concept of a solitary wave was introduced to science by John Scott Russell in 1844, when he observed a wave which was formed when a rapidly drawn boat came to a sudden stop in narrow channel [5]. These waves, now called solitons, have become important subjects of research in diverse fields of physics and engineering. Well know general references on solitons are [6]–[8]. Soliton based technologies have been investigated in detail in the field of Optics since a pioneer work on Solitons in optical fibres [9].

A large amount of efforts were spent during the eighties and early nineties to obtain record distances of optical solitons [10]. In 1998, T Georges and his team at France Télécom R&D Center, combining optical solitons of different wavelengths (wavelength division multiplexing), demonstrated data transmission of 1 Tb/s over 1000 km of standard fiber with 100 km amplifier spans [11].

Papers focused on possible applications of solitons to the field of Electronics are more scarce [12], [13]. In this field the base solution for soliton propagation in a non linear

transmission line (NLTL) is used to optimize the line equivalent inductance and capacitance in order to obtain the desired waveforms.

An important related application is pulse sharpening for non return-to-zero (NRZ) data transmission in digital circuits, by improving the edges of the pulses. Improving the transitions by shrinking the rise and fall times of pulses can be useful in other applications, such as high-speed sampling and timing systems. Sharpening of either the rising or falling edge of a pulse has been demonstrated on a GaAs technology [14]. Feasibility of simultaneous reduction of both rise and fall times was demonstrated by two Caltech researchers, Afshari and Hajimiri [15].

The basic idea for pulse generator design consists in feeding a NLTL with a conventional, low bandwidth pulse generator and using this line to reduce the rise and fall times, which results into a narrowing of the pulse width. A pulse narrowing NLTL using Si MOS varactors and metal micro-strip transmission lines in a 0.18µm BiCMOS process is reported in [15]. An output pulse of 2.5 ps was obtained from simulation for a 65ps input pulse with a 1 V amplitude, although due to limitations in the experimental tests this compression could not be fully validated. One-port (output-only) electrical circuits that robustly self-generates a periodic, stable train of electrical soliton pulses with no high-frequency input were reported in [16] and [17].

A NLTL can be fabricated with a high-impedance waveguide periodically loaded with reactances exhibiting a non-linear dependence with bias voltage. One popular way of implementing these capacitances is by means of reverse biased diodes, as shown in Figure 2.5. The capacitances cause the propagation delay through the NLTL to depend on the wave amplitude. Nonlinearity arises from the voltage-dependent propagation characteristics of the NLTL, dispersion arises from their frequency dependence.

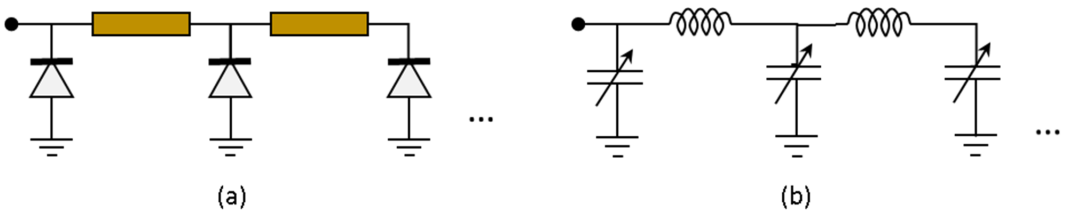

Figure 2.5 Non linear transmission line based on diodes (a) and equivalent circuit (b).

In the case of a weakly dispersive NLTL, the nonlinearity can counteract the normally present dispersive properties of the line maintaining solitary waves that propagate without dispersion. This behavior can be explained by considering the instantaneous propagation velocity at any given point in time and space, which is given by

$$v_p = 1/\sqrt{L/C} \tag{2.2}$$

In the presence of a nonlinear capacitor with a voltage dependence, the instantaneous capacitance can be smaller for higher voltages. Therefore, the points closer to the crest of the voltage waveform experience a faster propagation velocity and produce a shock-wave front, due to the nonlinearity. On the other hand, dispersion of the line causes the waveform to spread out. For a proper nonlinearity, these two effects can cancel each other out.

Due to the generation of the shock wave front, these generators are in some references called shock line generators. It is remarkable that the physical effect is the essentially the same that leads to the generation of the Cherenkov radiation, as pointed out by Grischkowsky in [18].

One issue in pulse narrowing NLTLs is that if the input pulse is wider than a certain minimum related to the natural pulse width of the line, the input pulse degenerates into multiple solitons. It is possible to solve this problem by using the gradually scaled nonlinear transmission lines proposed by Case in [12]. The concept is shown in Figure 2.6.

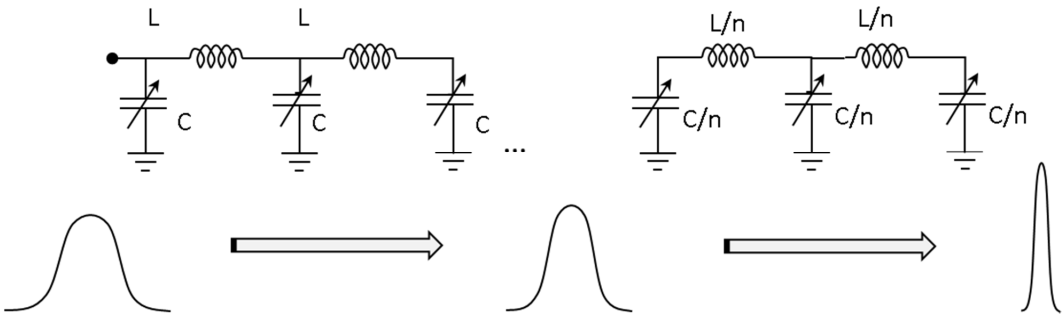

Figure 2.6 Waveforms in a gradually scaled non linear transmission line.

The first few segments have the widest characteristic pulse, meaning that their output is wider and has smaller amplitude. As a result, the input pulse will cause just one pulse at the output of these segments. The following segments have a narrower response and the last segment has the narrowest one. This will guarantee the gradual narrowing of the pulses and avoids degeneration. Each segment has to be long enough so that the pulse can reach the segment's steady-state response before entering the next segment.

Unfortunately, the NLTL architecture has inherent drawbacks. NLTL-based pulse generators generally have a very low jitter, but are complex to manufacture and do not suit the integration in low-cost monolithic ICs. On the other hand, achieving close agreement between the rising and falling edge speeds is challenging. Further, the shock line architectures commonly exhibit difficulties in impedance matching.

Due to these limitations, generators based on differential amplifiers are preferred for applications where differential square wave generation are needed [19]. The Keysight's

N2806A calibration generator uses differential amplifiers fabricated with Indium Phosphide HBT technology which can produce sub-7 ps fall times and sub-9 ps rise times [20].

NLTLs have been however very successful for the development of comb generators [21], [22]. A comb generator is essentially an oscillator that produces signals with multiple harmonics, ideally with the same amplitude, in a large frequency band. In the time domain this corresponds to a train of Dirac deltas. The name comes from the visualization of the signal in the frequency domain with a spectrum analyser.

The primary application for comb generators is as frequency multipliers to produce a high frequency phase-locked to the input. Generally, the harmonics are fairly stable with time and temperature. It is generally believed that the NLTL technology is superior over the conventional one based on Step Recovery Diodes, particularly in terms of Phase Noise [23].

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Chapter 3. Critical Figures of Merit

3.1 Pulse shape integrity

One of the most important issues that the electronic designer has to deal with is to guarantee the preservation of the signal quality throughout the entire circuit, where, especially at high speeds, undesirable transmission effects or mismatches can take place.

There are several factors that affect to the signal integrity, that most of the times they are closely related among them: attenuation in transmission lines, mismatches, crosstalk and ground bounce.

There exist a lot of interesting literature that can help the designer to a great extent when developing high speed circuits. In particular, it is worthy to highlight the work presented in [1], which is a review of the signal integrity and related issues of the past decades with more than a hundred of references. On the other hand, an useful high speed design guideline is that from Altera [2]. And finally, for further and more advanced information, the book [3] is a good reference for very high speed designs.

3.1.1 Transmission Lines

Usually, when working at low frequencies and with transmission line lengths not excessively long, there are not special undesirable effects to be aware of. However, at high frequencies, even the short distances of a PCB can have negative effects in the integrity of the transmitted signal.

The ideal transmission line can be modeled by just inductors in series and capacitors in parallel, without losses or frequency dependence. Its impedance is then $Z_0 = \sqrt{L/C}$. Nevertheless, in practice, there are many effects that distance the transmission line from ideal. Such effects are taken into account by adding series and parallel resistances, as shown in figure 3.1. The line impedance is now $Z_0 = \sqrt{(L+R)/(C+G)}$.

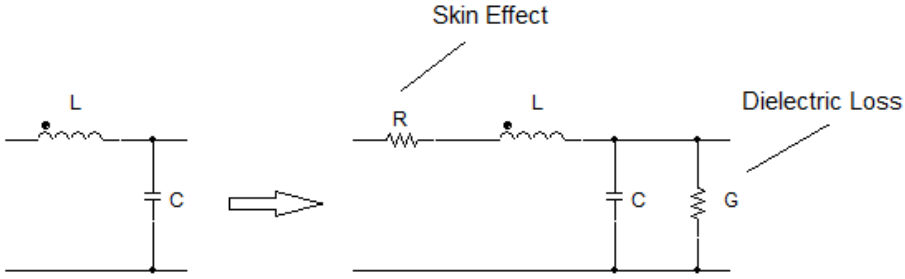

Figure 3.1 Lossless (left) and lossy (right) transmission lines

The series resistance is caused by the conductor resistance and the skin effect, while the parallel resistance is due to dielectric losses [4][5]. R and G are not constant but frequency dependent, having more influence as frequency increases. The conductor resistance results in a minor amplitude of the signal, while the skin effect and the dielectric losses cause a smaller bandwidth. Consequently, higher frequencies are attenuated to a greater extent than lower ones. In the case of a pulse, this is traduced in an increase of the signal transition times. Additionally, such variations in the impedance are the source of mismatches that cause the degradation of the original signal.

The losses in the line can be classified according to the frequency dependence: DC loss and AC loss. DC loss is due to the conductor ohmic resistance. On the other hand, AC loss is frequency dependent and there are two primary factors that cause the line impedance to increase with frequency: dielectric absorption and skin effect.

Dielectric absorption

At high frequencies, a part the propagating signal energy is absorbed in the dielectric substrate. The amount of losses is a function of the dielectric material. Consequently, for minimizing the dielectric absorption it is required to select a PCB substrate with a low loss tangent (tanδ).

Skin effect

Skin effect is the tendency of the high frequency signal to travel near the outer surface of the conductor [11]. The skin effect causes an increase of the resistance since the effective cross sectional area of the conductor is decreased. Because the skin effect is a function of frequency, consequently the conductor impedance is also a function of frequency. Then, high frequencies are more attenuated than lower ones, what affect to the signal integrity. Another undesirable consequence of skin effect is that the traces heat to a greater extent with high frequencies signals than with low frequency ones, for the same level of current.

The physical origin of skin effect is the following. At low frequencies the current is uniformly distributed throughout the conductor. But at high frequencies, the rapid changes in the current produce also rapid changes to its associated magnetic field. That varying field causes the generation of eddy currents [12] which reinforce the main current flow at the surface but are opposite to it toward the center. Consequently the current density is higher at the surface.

In order to estimate the effective cross sectional area of the conductor it is introduced the skin depth parameter, which is defined as the point where the current density has decreased to $J = J_0/e$. It can be approximated by,

$$\delta = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_r}} \tag{3.1}$$

In the above equation ρ is the resistivity of the conductor, f the frequency of the current, μ_0 the permeability of free space and μ_r the relative magnetic permeability. As it can be remarked, the skin depth is inversely proportional to the square root of the frequency (in Hertz). Likewise, it does not depend on the shape of the conductor.

The current density J in the conductor decreases exponentially from the surface toward the center,

$$J = J_0 e^{-d/\delta} \tag{3.2}$$

where J_0 is the current density at the surface, d the distance from the surface toward the center and δ the skin depth. It may be noted that a value of the skin depth greater than the center of the conductor means that it is not limited by skin effect and the current is almost uniformly distributed in the conductor. Consequently, thicker traces suffer from skin effect at lower frequencies than thinner ones.

Possible solutions to these effects is the use of Pre-Emphasis and receiver equalization [13][14]. There are more effects that play an important role, at high frequencies, to the signal losses, as:

- The surface roughness: due to the skin effect, the signal tends to travel close to the surface. When it is rough, it makes longer the path that the current has to travel, being increased then the signal losses.

- Proximity effect: the mutual inductance between the trace carrying the signal and the ground plane (signal return) causes the signal current density to concentrate the closest to the ground plane. That increases to a greater extent the conductor resistance.

3.1.2 Mismatches

Different values of the impedance of the source, the line and the load cause the generation of signal reflections as a consequence of the impedance mismatching [6]. Consequently, the signal is not completely transmitted and the reflected part continues back and forth until all energy is absorbed and signal vanishes. The consequences of that are signal overshoot, undershoot, ringing and stair-step waveforms.

In a PCB design, there are several elements that cause the alteration of the inductance or capacitance of the transmission line. That produces a change on the line impedance and consequently reflections. Examples of impedance disturbance sources are the vias, trace bends, pads and connectors. Regarding the vias, used for interconnecting layer, there are three different kinds used in PCB design: through hole, blind and buried vias [7]. Due to its influence on signal integrity, high frequency vias models have been widely studied, see for instance [8], [9] or [10].

3.1.3 Crosstalk

Another known undesirable effect that arises in common PCBs layouts is crosstalk. Due to the proximity among traces, unintended electromagnetic coupling can take place, both inductive (magnetic field) and capacitive (electric field). Some ways to minimize crosstalk is separating as much as possible the traces with different type of signals or using ground planes to shield the sensitive areas.

An exhaustive analysis about crosstalk and some other processes that affect to the signal integrity is performed by R. P. Clayton in [15]. On the other hand, in [16] it is proposed the use of serpentine guard trace vias for suppressing both far-end (FEXT) and near-end crosstalk (NEXT).

3.1.4 V_{CC} & Ground bounce

Ground bounce is a source of noise and signal distortion caused by the parasitic inductance of the lead connected to the ground at high frequencies [17][18]. When sudden changes in the current toward the ground occur, a voltage spike is generated across the inductance, causing the internal ground to be at a different potential than the external ground. Current spikes are commonly caused by fast transition times, being the ground bounce more significant as shorter are the transition times and greater the inductance values. A similar problem occurs in the supply voltage (Vcc bounce), usually of lesser interest since the signal are referenced to ground and not to the supply voltage.

The total lead inductance is composed by the internal package inductance (internal connections) plus the inductance of the connection from the package pins to the external ground (PCB planes or traces). Two ways for reducing the ground bounce are: to place bypass capacitors as close as possible of the device and make the traces as short as possible for minimizing inductances.

This problem is specially critic in devices with a large number of I/O (for instance FPGAs), since the switching of much of them at the same time can aggravate ground bounce. For that reason, such devices usually have a Simultaneous Switching Outputs (SSO) limit.

3.2 Noise

The noise can be defined as the spontaneous fluctuation in current or in voltage, and it is present in all semiconductor devices. In this section the most relevant parameters for measuring the quantity of noise and the most important sources of noise are analyzed.

3.2.1 Figures of merit

Very useful parameters that indicate the quantity of noise in a system are the signal to noise ratio and the noise figure. The first of them is defined as the ratio of power of a signal and the power of the noise, and it is commonly expressed in decibels:

$$SNR(dB) = 10log\left(\frac{P_{signal}}{P_{noise}}\right) \tag{3.3}$$

It is defined v(t) and i(t) as the deterministic voltage and current values (i.e. the signal), and e(t) and j(t) as their respective voltage and current random values (i.e. the noise). Assuming a similar impedance for both signal and noise, the above equation can be expressed in terms of voltages or currents:

$$SNR(dB) = 10log\left(\frac{V_{rms}^2}{E_{rms}^2}\right) = 20log\left(\frac{V_{rms}}{E_{rms}}\right) = 20log\left(\frac{I_{rms}}{J_{rms}}\right) \tag{3.4}$$

where V_{rms}, E_{rms}, I_{rms} and J_{rms} are the respective root mean squares (RMS) of the waveforms v(t), i(t), e(t) and j(t). A very important property of the RMS it that its value is not zero even if the average of the signal is.

As it can be remarked, the SNR is desirable to be as great as possible, in order to have values of the signal much larger than the noise. On the contrary, a value of 0 dB of the SNR implies that it is not possible to discriminate between the signal and the noise. Of course, the signal to noise ratio can be also expressed in linear units. For example for a voltage signal it yields,

$$SNR(linear) = \frac{V_{rms}^2}{E_{rms}^2} \tag{3.5}$$

The second parameter that characterizes the noise on a system is the noise factor. It was introduced in 1944 by Harald T. Friis [19] and it is defined as the ratio between the SNR at the input (SNR_i) and at the output (SNR_o) of a certain network.

$$F(linear) = \frac{SNR_i(linear)}{SNR_o(linear)} \tag{3.6}$$

$$F(dB) = \frac{SNR_i(dB)}{SNR_o(dB)} \tag{3.7}$$

When the noise factor in linear units is expressed in decibels, it is called noise figure:

$$NF(dB) = 10log\big(F(linear)\big) = 10log\left(\frac{SNR_i(linear)}{SNR_o(linear)}\right) \tag{3.8}$$

The noise factor, or the noise figure, measures the level of degradation that a device introduces in the signal to noise ratio (SNR). The ideal system is that one which does not

generate any noise, and presents a value of the noise figure of 0 dB (F=1). It is important to remark that this does not mean zero noise level at the output, but that the noise contribution to the system comes exclusively from the noise present at the input. That is, for example in the case of an amplifier, the input noise is multiplied by the gain of the device and consequently the noise at the output is greater than at the input. However, as the input signal is multiplied by the same transfer function, it is amplified in the same way and the SNR is preserved. In practice, all the circuits add noise to the system so the SNR at the input is always greater than at the output. A Monte Carlo simulation of the noise injected to a pulse by amplifiers and matching pads can be found in Appendix B.

Correlated noise sources

In usual situations there is not just one source of noise but there are some of them algebraically superimposed. These noises may depend on each other but also can be statistically independent (not correlated). In the case there are two noise signals $e_1(t)$ and $e_2(t)$, the RMS of the resultant noise E_{rms} yields,

$$E_{rms}^2 = \overline{e_t^2(t)} = \frac{1}{T}\int_0^T [e_1(t) + e_2(t)]^2\, dt = \frac{1}{T}\int_0^T [e_1^2(t) + e_2^2(t) + 2e_1(t)e_2(t)]\, dt \qquad (3.9)$$

The integral averaging of the first and the second term of the rightmost expression of (3.9) correspond to the individual mean square values of the noise voltages $e_1(t)$ and $e_2(t)$, respectively.

It is introduced the correlation coefficient c, which is defined as [20],

$$c = \frac{\frac{1}{T}\int_0^T e_1(t)e_2(t)\, dt}{E_{1rms}E_{2rms}} \qquad (3.10)$$

where $-1 \leq c \leq 1$. A value of $c = 0$ implies that the two noise signals are uncorrelated, which means that they are caused by different physical processes. On the other hand, a value of $c = \pm 1$ implies maximal correlation between the signals. Substituting equation (3.10) into (3.9) yields,

$$E_{rms}^2 = E_{1rms}^2 + E_{2rms}^2 + 2cE_{1rms}E_{2rms} \qquad (3.11)$$

Then, for uncorrelated signals, the mean squared value of the total noise is the sum of the mean squared values of the individual signal noises. The above expressions can be easily extrapolated to noise currents by just substituting voltages by currents.

3.2.2 Noise sources

The inherent noise present in all semiconductor devices is the result of the superposition of different noise sources. The most important noise sources are thermal noise, shot noise, flicker noise, generation-recombination, $1/f^2$ noise, burst noise and avalanche noise.

Each type of noise has a particular behavior against frequency, so analyzing the spectral response of a system can help to a greater extent to have a better idea about the sources of noise that most affect to it. In particular, when the spectral power density of the noise is independent of frequency, i.e. flat response, it is called withe noise. Examples of withe noise are the thermal and the shot noise.

3.2.2.1 Thermal noise

Also called Johnson noise or Nyquist noise, it is generated by the random motion of charge carriers due to the thermal excitation. Thermal noise was firstly discovered and experimentally measured by J. B. Johnson [21] and theoretically explained next by H. Nyquist [22]. The most important aspects of this type of noise are the next:

- It is present in all conductors and is one of the most common sources of noise in electronics.
- It is independent of the applied voltage or the current flow.
- It has a Gaussian amplitude distribution in the time domain.
- Devices with just reactive component do not produce thermal noise.
- The thermal noise establishes the minimum level of noise that can be achieved in a system at a certain temperature.

The value of the Johnson noise in terms of voltage, current and power is determined by the following equations:

$$P_{thermal}(rms) = 4kT\Delta f \tag{3.12a}$$

$$E_{thermal}(rms) = \sqrt{4kTR\Delta f} \tag{3.12b}$$

$$J_{thermal}(rms) = \sqrt{\frac{4kT\Delta f}{R}} \tag{3.12c}$$

Where k is the Boltzmann's constant ($1.38 \cdot 10^{-23} J/K$), T the absolute temperature in K, R the resistance and Δf the frequency bandwidth.

From the above equations it is shown that thermal noise is proportional to temperature and bandwidth. Consequently the way to minimize this type of noise is mainly performed by cooling the circuit and reducing the system bandwidth. It is also extracted that thermal noise power density is independent of frequency, as it yields $dP_{thermal}/df = kT$. Thus, it is white noise.

3.2.2.2 Shot noise

Shot noise, or Schottky noise, results from the flow of current across a potential barrier. Due to the fact that the current is not continuous but consists of a flow of discrete charges, random fluctuations in the current flow are originated. Shot noise comes determined by the following equation,

$$J_{shot}(rms) = \sqrt{2qI\Delta f} \tag{3.13}$$

where I is the forward junction current and q the electron charge. The noise is proportional to the pass of current through the device and independent of the temperature, in contrast with thermal noise. On the other hand, it is also white noise. The noise spectral density function of the equivalent current yields,

$$\frac{dJ_{shot}^2}{df} = 2qI \tag{3.14}$$

Because of the small value of the *q* charge, this type of noise is almost insignificant in a wide number of cases, where thermal and flicker noises constitute the largest part of the total noise. Nevertheless, there are other cases where it is not negligible. Shot noise is independent of the temperature and frequency. On the contrary the flicker noise decreases with frequency and thermal noise does the same with temperature. Consequently, at high frequencies and low temperatures shot noise may become the dominant source of noise.

Examples of devices that suffer this type of noise are the diodes, transistors and vacuum tubes. Even if is widely instilled that the shot noise is not present is resistors, new studies demonstrate that this affirmation could be incorrect [23].

3.2.2.3 1 / f noise

The 1/f noise (one-over-f) is also known as contact noise, pink noise or flicker noise, and it is present in all semiconductor devices under biasing, as well as in a wide variety of natural phenomena. Some examples are shown in Figure 3.2. The origin of this type of noise is still an active area of research and there is not an universal equation to calculate it. In fact, it depends on the device and there are usually several mechanisms involved in its generation. This noise features a spectral power density inverse to the frequency:

$$S(f) = \frac{constant}{f} \tag{3.15}$$

At low frequencies this is the dominant source of noise, while at high frequencies it is negligible. For that reason DC measurements require for high technology instrumentation in order to achieve accurate results.

A characteristic parameter that determines the flicker noise is the corner frequency, which is defined as the point where the 1/f noise is equal to the white noise (see Figure 3.3).

One of the most extended models for the flicker noise in semiconductors and metals is the bulk model proposed by Hooge [25][26], who defends that the 1/f noise is a fluctuation in mobility and that it is encountered in the lattice scattering. The 1/f noise can be determined by the following empirical relation:

$$\frac{S_V(f)}{V^2} = \frac{S_I(f)}{I^2} = \frac{S_G(f)}{G^2} = \frac{S_R(f)}{R^2} = \frac{\propto_H}{N_C f} \tag{3.16}$$

where S_X is the spectral power density of the fluctuations in the parameter X (voltage, current, conductance or resistivity), $\propto_H$ the Hooge parameter and N the total number of moving charges (electrons or holes).

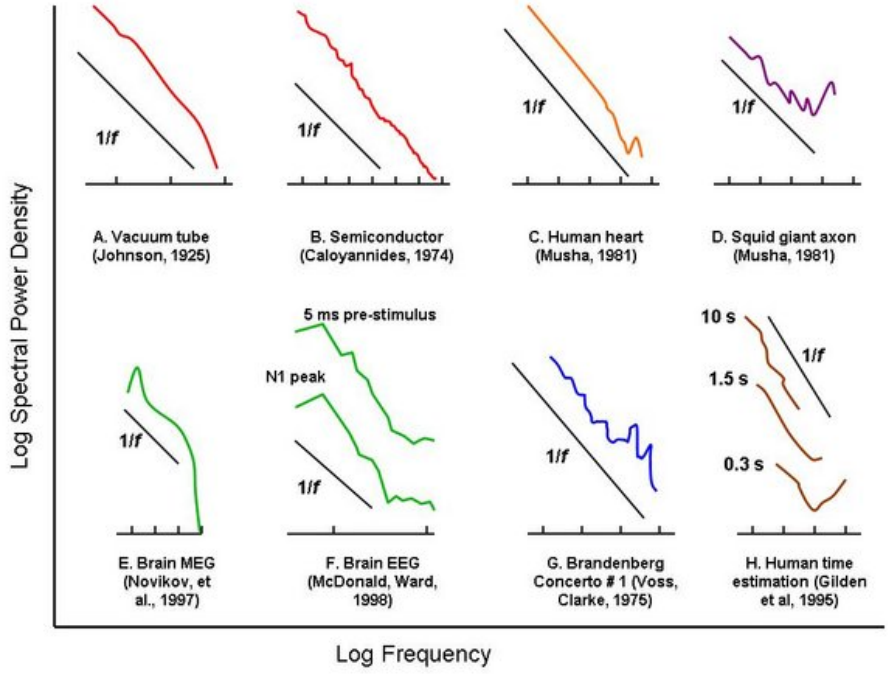

Figure 3.2 Examples of 1/f noises [24]

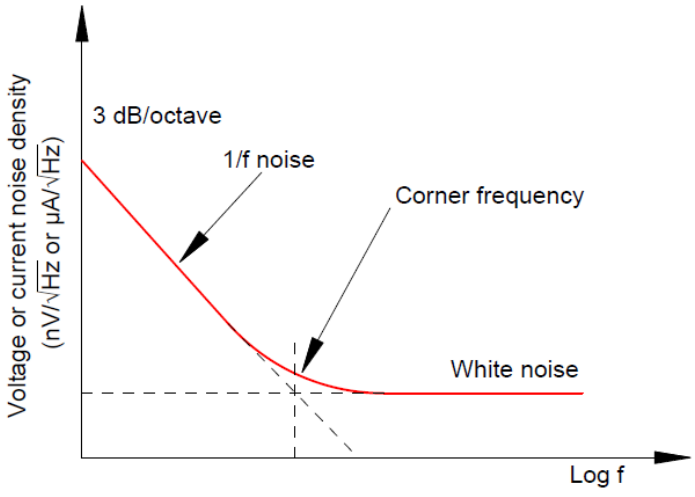

Figure 3.3 Corner frequency

The value of $\propto_H$ was firstly thought to be constant, with a value of $2 \cdot 10^{-3}$, but further experiments have demonstrated that it is not constant but variable and dependent on the material [27]. Imperfections of the crystal lattice mean high 1/f noise, while a perfect crystal lattice implies very low $\propto_H$ values.

There exist others hypothesis, as the surface model of McWhorther [28]. In this theory it is proposed that the 1/f noise is caused by the fluctuation in the occupation of the surface traps, what can alter the conductivity. An unified model of the Hooges' and McWhorther's proposals for MOSFETs can be can be found in [29].

3.2.2.4 Generation-Recombination

Generation-Recombination noise is caused by the statistical fluctuation in the number of carriers due to the existence of generation-recombination centers. It was first introduced by Van Vliet and Blok [30] and deeply described later by Van Vliet and Fassett [31]. The spectral density function of the GR noise is given by,

$$\frac{S_R(f)}{R^2} = \frac{S_G(f)}{G^2} = \frac{S_N(f)}{N_0^2} = \frac{\overline{\Delta N^2}}{N_0^2} \frac{4\tau}{1 + (2\pi f \tau)} \tag{3.17}$$

where $S_R(f)$, $S_G(f)$, $S_N(f)$ are the spectral density of resistance, conductance and carrier number, respectively, $\overline{\Delta N^2}$ is the variance of the number of carriers, N_0 is the average of the number of carriers and finally τ is the carrier lifetime. A detailed analysis of GR noise has been carried out by V. Mitin, L. Reggiani and L. Varani, whose work can be found in the Chapter 2 (*Generation-Recombination Noise in Semiconductors*) of the compilation book edited by A. Balandin [32].

3.2.2.5 $1/f^2$ noise

This kind of noise is due to a dc-current induced resistance drift and for observing it high current densities are needed. Electromigration is one of the most important, or at least most interesting, physical process that gives rise to $1/f^2$ noise. The spectral density of the voltage noise can be written as,

$$S_V(f) = \frac{I^\beta C}{f^\gamma T} e^{-E_a/kT} \tag{3.18}$$

where $\beta \geq 3$, $\gamma \geq 2$, C is a parameter that depends on geometry and technology, *k* is the Boltzmann constant and E_a is the electromigration activation energy. The $1/f^2$ noise is widely used in the diagnosis of metal interconnections of integrated circuits [33], where high current densities exist due to the reduced space of the connections.

3.2.2.6 Burst Noise

Burst noise is another type of low frequency noise which is believed to be caused by charge traps or microscopic defects in the semiconductor. The capture/emission of the carriers causes the random switching between several (commonly two) discrete values (Figure 3.4). Burst noise becomes more pronounced in smaller devices and at low frequencies. It is also called random telegraph signal (RTS), because it resembles telegraph signals, and popcorn noise, because of the sound it makes when listened over a speaker. The current power spectral density is given, according to [34][35], by

$$S_{RTS}(f) = \frac{4(\Delta I)^2}{(\overline{\tau_l} + \overline{\tau_h})[(1/\overline{\tau_l} + 1/\overline{\tau_h})^2 + (2\pi f)^2]} \tag{3.19}$$

where ΔI is the amplitude of the RTS signal, and $\overline{\tau_l}$ and $\overline{\tau_h}$ are the average times in the RTS pulse low (emission time) and high (capture time) levels, respectively:

$$\overline{\tau_l} = \frac{1}{P}\sum_{i=1}^{P} \tau_{l,p}; \overline{\tau_h} = \frac{1}{S}\sum_{i=1}^{S} \tau_{h,s} \tag{3.20}$$

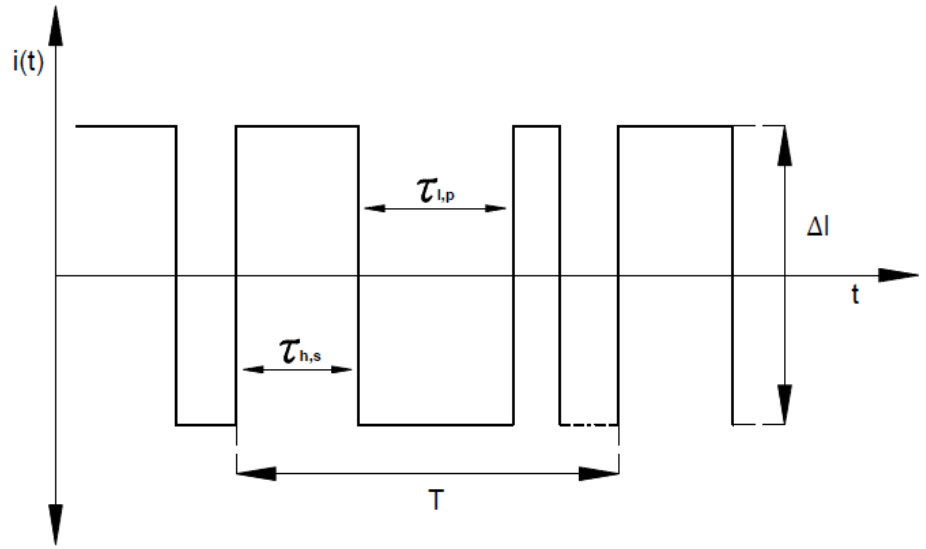

Figure 3.4 RTS noise

3.2.2.7 Avalache Noise

Avalanche noise is caused by carrier multiplication in a reverse biased p-n junction. When the electric field in the space charge layer is very high, the carriers are accelerated and their energy is increased. Consequently when they collide with the lattice they are able to generate electron-hole pairs. These new pairs will be also accelerated and will collide producing additional pairs of carriers. This is referred to as avalanche multiplication and if it

is not controlled can lead to the breakdown of the p-n junction, resulting in large reverse currents. The current spectral density is normally expressed as [36],

$$\overline{J_{av}^2} = 2qI\overline{M^2}\Delta f \tag{3.21}$$

where I is the reverse biasing current and M the amplification factor. The magnitude of the noise is difficult to predict since depends on the material. In comparison with shot noise, avalanche noise is much greater for a similar current. Finally, as deduced from (3.21), the spectrum of avalanche noise is white.

3.2.3 Modeling noise in particular devices

In this section it is analyzed the different kind of noises that arises in the main devices used along this thesis. That is, resistors, diodes and MOSFETs.

3.2.3.1 Resistors

The resistor is the most basic case of white noise. In particular, of thermal noise. The real resistor can be modeled as a noiseless resistance R in series with the noise voltage (Thevenin representation) or in parallel with the noise current (Norton representation), as shown in Figure 3.5.

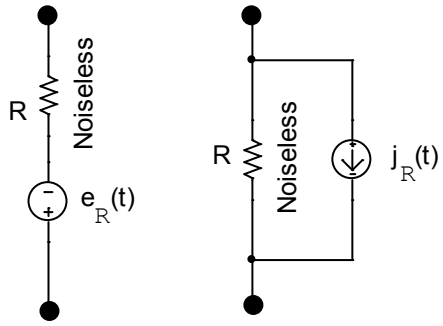

Figure 3.5 Resistor noise model. Left: Thevening topology. Right: Norton topology

The value of the thermal noise in terms of voltage of a resistance R is determined by the next equation,

$$\overline{e_R^2(t)} = 4kTR\Delta f \tag{3.22}$$

which is present even if the circuit is not under bias. For representing the thermal noise in terms of current it is just needed to divide the equation (3.22) by R^2,

$$\overline{J_R^2(t)} = \frac{\overline{e_R^2(t)}}{R^2} = 4kTG\Delta f \tag{3.23}$$

where G is the conductance.

3.2.3.2 Diodes

The main source of noise in a diode is the shot noise, which is dependent on the current, as opposed to the thermal noise. For that reason this noise is present when the diode is forward biased. This kind of noise may be represented indifferently in terms of voltage or current, but is most common to use the noise equivalent current model, as shown in figure 3.6. Consequently for a value of the current I through the diode, it yields,

$$\overline{j_D^2(t)} = 2qI\Delta f \tag{3.24}$$

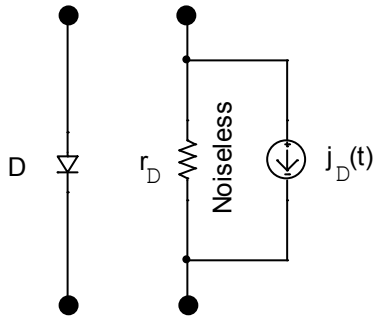

Figure 3.6 Diode noise equivalent model under forward biasing

3.2.3.3 MOSFETs

In MOSFETs, the two major noise sources are the 1/f noise and the thermal noise, but some others also take place. The most relevant are the drain current thermal noise caused, the induced gate noise and the drain flicker noise.

Drain Current Noise

This noise is originated because of the resistive channel between the drain and the source. When the transistor operates in the ohmic region, the total noise is mainly composed by thermal noise. When it enters in the saturation region, there is a mix of thermal noise with a small component of shot noise.

For the calculation of the drain current noise the channel cannot be treated as an homogeneous resistor. Such assumption would be only correct in the case the drain to source is $V_{DS} = 0$. However, in normal operation where $V_{DS} \neq 0$, the channel presents higher conductivity in the source that in the drain.

For that reason an analysis considering the entire channel composed by multiple segments in series of resistance ΔR is required (Figure 3.7). This is the so called channel segmentation

model. As it can be observed there is an associated capacitance towards the gate at each segment. Later will be shown that this capacitance is responsible of the noise gate.

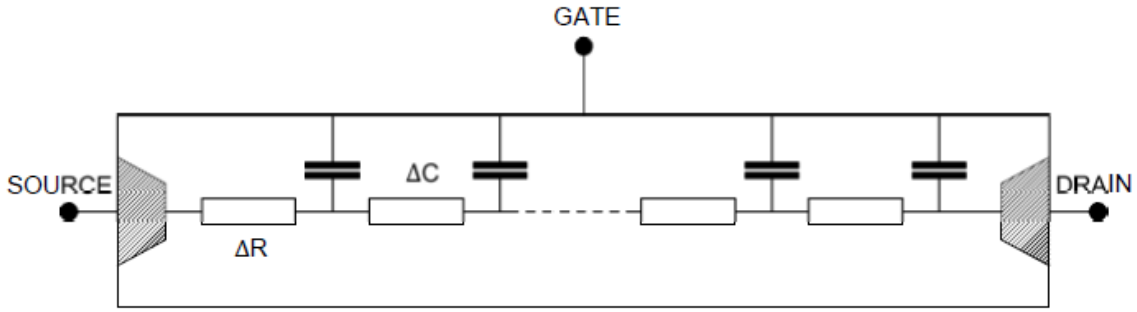

Figure 3.7 Channel segmentation model

It is obtained that the drain current noise in a Field Effect Transistor is determined by the following equation [37]:

$$\overline{j_{th\_d}^2(t)} = 4kT\gamma g_m \Delta f \tag{3.25}$$

where g_m is the transconductance of the transistor in saturation and γ the white noise gamma factor. The factor γ depends on the type of device, on its channel length and on its working region. It is usually between 2/3 and 1. For example, for a MOSFET in the linear region it has a value of $\gamma = 1$, while in the saturation region it can be approximated to 2/3.

The value of the transconductance in saturation is obtained by means of the following expression, which coincides with the value of the conductance g_{d0} when $V_{DS} = 0$:

$$g_m = \mu_C C_{OX} \left(\frac{W}{L}\right)(V_{GS} - V_T) \tag{3.26}$$

where C_{OX} is the gate oxide capacitance per unit area, W the channel width, L the channel length, V_{GS} the gate to source voltage, V_T the threshold voltage and finally μ_C the free carrier mobility (that is, electron mobility μ_n for n-channel transistors and hole mobility μ_n for p-channel transistors).

An important remark that can be extracted from the above equations is that the drain current noise is greater in NMOS than in the homologue PMOS transistor, as the electron mobility is greater than the hole mobility.

Gate noise

The gate noise is composed by the fluctuations in the channel that are introduced to the gate (induced gate noise) and, to a lesser extent, by the thermal noise due to the physical

resistance of the gate. The induced current gate noise is due to the capacitive coupling between the channel and the gate and is expressed as [38][39],

$$S_{j_g} = 4kT\beta g_g \tag{3.27}$$

where,

$$g_g = \frac{w^2 C_{GS}^2}{5g_{d0}} \tag{3.28}$$

and a value of $\beta = 4/3$ has been measured for long channel MOSFTs. This noise is specially significant at high frequencies, since it is proportional to f^2. Since the induced gate noise derives from the thermal channel noise, it is expected that both noises are correlated, as actually they are [40].

On the other hand, the withe thermal noise modeled as a voltage in series with the gate resistor, is determined by

$$\overline{e_{th\_g}^2(t)} = 4kTR_g\Delta f \tag{3.29}$$

Drain flicker noise

The 1/f noise is especially prominent in MOSFETs. As previously commented, the origin of the flicker noise is still an open issue and there are mainly two theories proposed: the mobility fluctuation model and the carrier number fluctuation model. It is also included the combination of both mechanisms.

Within these theories the mean square value of the drain flicker noise current can be calculated by means of the following expression [41][42],

$$\overline{j_{f\_d}^2(t)} = \left(\frac{K_f}{f}\right)\left(\frac{g_m^2}{WLC_{OX}^n}\right)\Delta f \tag{3.30}$$

where the parameters K_f depends on the model, that is:

- In the case of the number fluctuation model, K_f is independent of the bias and n=2.

- In the case of the mobility fluctuation model, K_f is a function of V_{GS} and n=1

The FET transistor that most suffers from flicker noise is the n-MOSFET, while the less affected by this kind of noise is the p-JFET.

The drain flicker noise can also be modeled as a voltage source in series with the gate, by simply dividing it by g_m^2,

$$\overline{e_{f\_d}^2(t)} = \left(\frac{K_f}{f}\right)\left(\frac{1}{WLC_{OX}^n}\right)\Delta f \tag{3.31}$$

Figure 3.8 shows the equivalent noise model of the MOSFET.

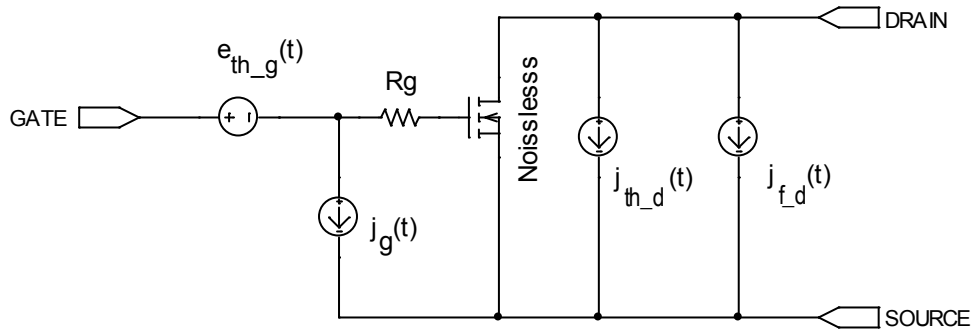

Figure 3.8 MOSFET noise model

There are other sources of noise that, to a lesser extent, contribute to the total noise of the MOSFET:

- The resistance of the substrate is not zero and consequently causes thermal noise.

- In highly scaled MOSFETs, RTS becomes a significant source of noise [43], [44].

- Gate leakage current gives rise to shot noise,

$$S_{I_G} = 2qI_G \tag{3.32}$$

- Induced flicker noise: in the same way the thermal channel noise ($\propto f^0$) gives rise to an induced gate noise ($\propto f^2$) by means of the capacitive coupling between gate and channel, the drain flicker noise ($\propto f^{-1}$) leads to an induced gate noise proportional to the frequency [38]. This noise does not have an important contribution to the total noise because at the frequencies where the flicker noise is dominant (low frequencies) the capacitive coupling between channel and gate is very small. Likewise, at high frequencies it is masked by thermal noise.

3.3 Jitter

Jitter is defined as the variation of a signal with respect to its ideal position in time. It is composed of both deterministic and random content [45]. The deterministic component is always bounded in amplitude and has specific causes, as they can be power supply noise, cross talk or EMI (Electromagnetic interference) radiation, spurious signals and sub-harmonics. On the other hand, random jitter is unbounded and comes from many sources, as thermal noise, shot noise, imperfections due to semi-regular doping density through semiconductor substrate, imperfections due to process anomalies, cosmic radiation, etc…

Random jitter can be characterized by a Gaussian distribution. That is, if many time measurements (for example of the period of a signal) are made and represented in an histogram, a Gaussian distribution will be obtained (Figure 3.9). The Jitter is usually quantified using the standard deviation of this distribution. As it can be observed in figure, the interval between ±σ would contain, approximately, 68.2% of all measurement taken, the interval ±2σ would contain 95.44%, the interval ±3σ would contain 99.74%, etc.

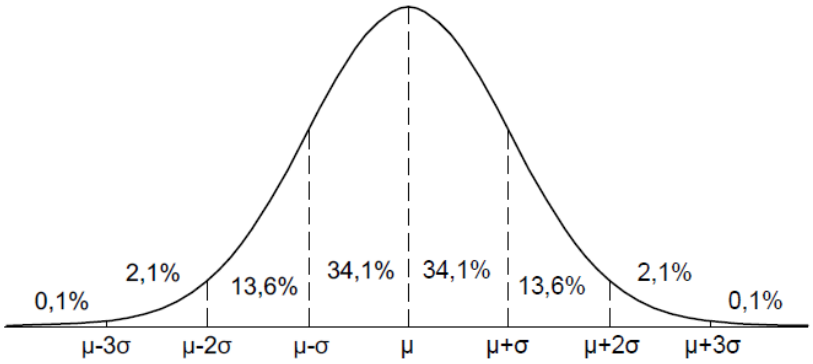

Figure 3.9 Gaussian distribution

As deterministic jitter is considered bounded, it is measured in terms of a peak-to-peak value (difference between maximum and minimum values). In contrast, random jitter does not have theoretically limit and will grow over time [46]. For that reason the standard deviation is used, as mentioned above. Total Random Jitter (RJ) is then:

$$RJ = N \cdot \sigma \tag{3.33}$$

where N is used to set a boundary and indicates the number of standard deviations used (Figure 3.9).

If there is just random jitter then the histogram will present just one peak. If there is also deterministic jitter (DJ) then there will be multiple peaks. Total Jitter is a linear combination of Random Jitter and Deterministic Jitter:

$$TJ = RJ + DJ = N \cdot \sigma + DJ(peak\ to\ peak) \tag{3.34}$$

Figure 3.10 shows the way for analyzing total jitter. As it can be observed, deterministic jitter is calculated by means of the difference between the means values associated with the far left and right Gaussian distributions. Likewise, random jitter is obtained from the standard deviations of the same left and right distributions.

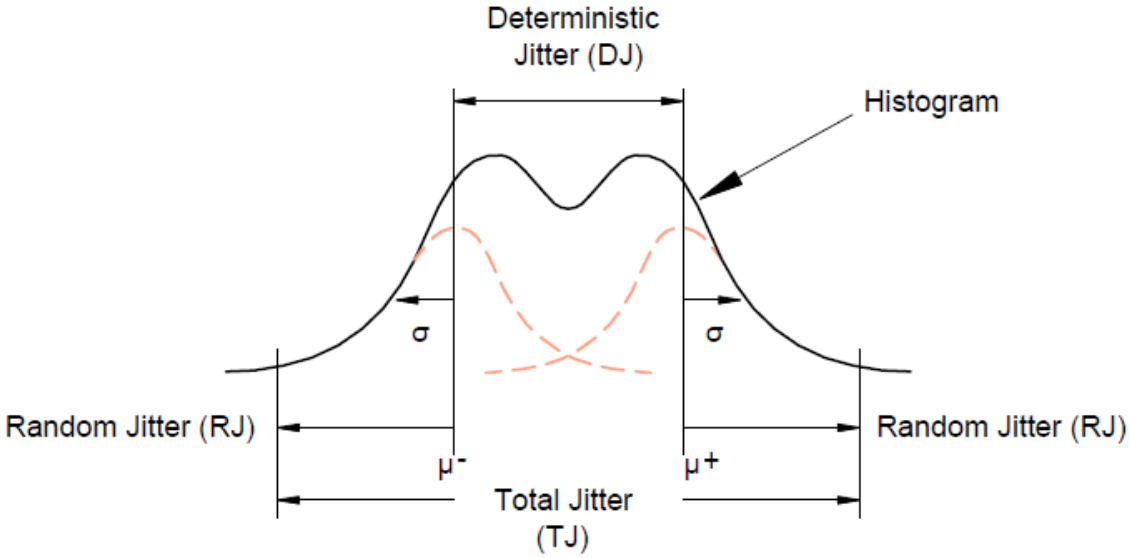

Figure 3.10 Total jitter analysis

3.3.1 Time domain

There are several ways in which jitter may be measured [47]:

- ***Period jitter***: it is defined as the time difference between a measured cycle period and the ideal cycle period (P1, P2 and P3 in Figure 3.11). It is the most popular way of measuring jitter. Usually, due the difficult to quantify the ideal period, the average period is treated as the ideal period. Like that, this type of jitter can be measured by means of an oscilloscope by triggering at a rising edge and measuring the jitter at the next rising edge.

- ***Cycle to cycle***: it is the time difference between two adjacent clock periods. As it can be noticed, there is no reference to an ideal cycle, so it is not needed to know the ideal edge location. It is showed in Figure 3.11 as C2 and C3.

A generalization of the above definitions is the accumulated jitter (also named long-term jitter), which comprise several cycles instead of just one.

- ***Time interval error (TIE)***: it is defined as the time difference between the ideal edge and the actual edge (measurements TIE1 through TIE4 in Figure 3.11), so in this case ideal edges must be known or estimated.

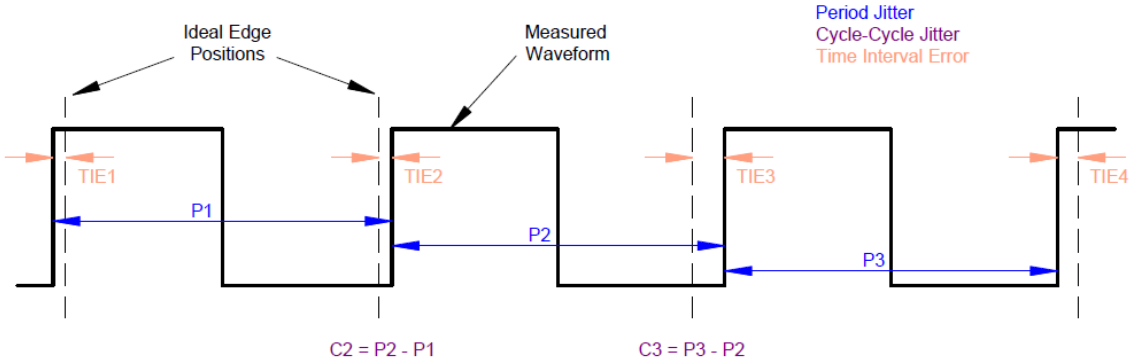

Figure 3.11 Time Domain Jitter Measurement

3.3.2 Frequency domain

Despite the most common measurement jitter is performed in the time domain, frequency domain may also be used, as jitter can be viewed as scaled phase noise. That is, for a sinusoid [48][49]:

$$\left.\begin{aligned} Jitter: V = Asin\left[2\pi f\left(t+\delta(t)\right)\right] \\ Phase\ Noise: V = Asin[2\pi ft + \alpha(t)] \end{aligned}\right\} \quad \delta(t) = \frac{\alpha(t)}{2\pi f} \tag{3.35}$$

As a result, instead of obtaining an ideal delta in the frequency domain, the power spectrum density $S(f)$ of Figure 3.12 will be observed. This spectral shape is determined by the probability distribution of the random variable α. The phase-noise spectrum $L(f)$ is defined as the attenuation in dB from the peak value of $S(f)$ at f_C to a value of $S(f)$ at f.

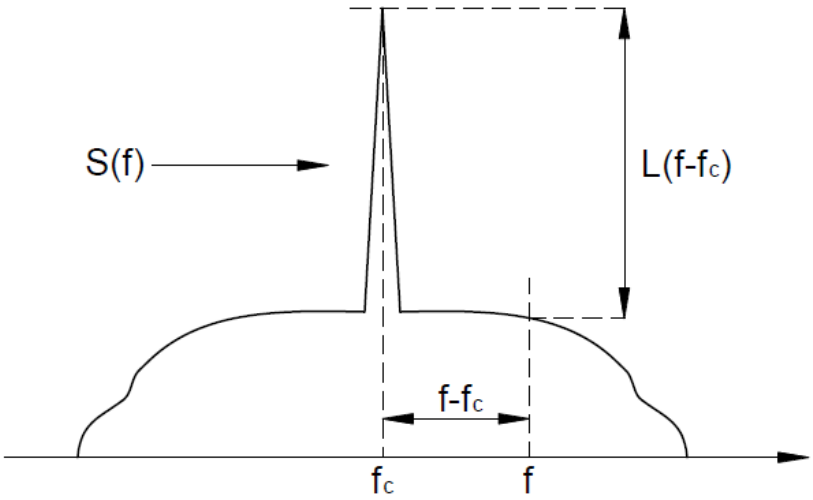

Figure 3.12 Spectrum of a signal with phase noise

Finally, in view of the fact that a square clock signal has the same jitter behavior as that of its base harmonic sinusoid signal [50], the possibility of measuring the jitter in the frequency domain is demonstrated, just analyzing the phase modulation of its first harmonic.

3.3.3 Jitter measurement instrumentation

Jitter can be measured using several instruments. The most usual are the Oscilloscopes, Time Interval Analyzers and Spectrum Analyzers (in particular the Phase Noise Analyzers). There are also dedicated instruments as Jitter Analyzers, or Bit Error Rate Testers (BERTs) for testing the quality of signal transmission in digital communication systems.

Throughout this thesis an oscilloscope is going to be used for jitter measurements, which is probably the most common instrument at laboratories. When working with this type of instrumentation it is crucial to take into account the jitter noise floor (JNF), which determines the outermost limit to which the signal jitter can be measured under optimal conditions. Some procedure to measure jitter using a real time digital oscilloscope can be found at [51].

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Chapter 4. SRD Pulse Generators

4.1 Introduction

The prototypes described in this chapter were used for testing the receiver boards of the MAGIC II telescope, the readout electronics of the MAGIC upgrade and proposed for testing the readout boards of the CTA largest telescope (LST).

Figure 4.1 shows the block diagram of the first prototype, aimed at testing the receiver boards of MAGIC II. Pulses in excess of 4 V were necessary in order to cover the full dynamic range of the VCSELs. As well, the designers of the receiver boards at the IFAE set the optimum pulse width of the order of 1 ns FWHM. Finally low noise, low jitter and minimum ringing were indispensable features.

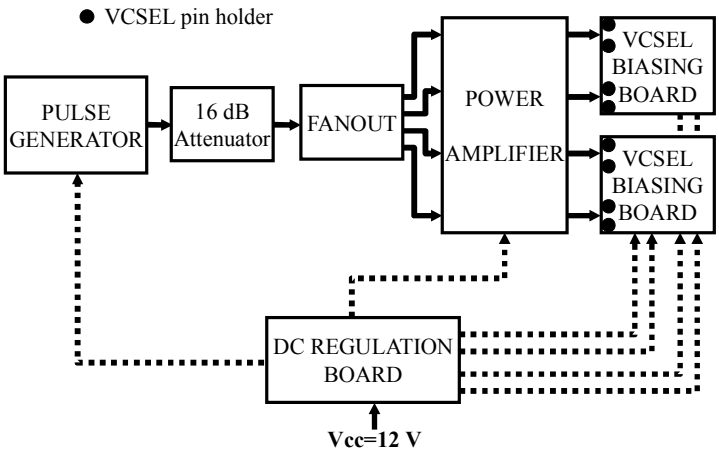


Figure 4.1 Four channel pulser block diagram

The pulse generator designed for this prototype was able to comply with the required specifications, with FWHM of 1.3 ns. The signal is split in four channels. Due to the power loss produced in this stage, the output has to be amplified. Two high bandwidth and high gain inverter amplifiers per channel compose the amplification board. An attenuator is placed before the fanout board in order to prevent the saturation of the amplifier. The pulses are next transmitted to two VCSEL biasing boards, which drive the VCSELs with a stabilized DC current source. Finally, a DC power board supplies the needed bias to all the active devices from a single 12 V source.

This prototype was the main accomplishment among all the SRD designs described in this Chapter, since the others, although with better performance, were essentially improved or slightly modified versions of this one. Therefore, this first prototype will be described in

detail along this chapter. The basis and major design issues of the main stages are described in Sections 3-5. The design of the particular boards required for the testing of the MAGIC II receiver boards and the physical implementation of the prototype is described in Section 6. And finally Section 7 is devoted to the last versions used for the MAGIC upgrade of the readout boards, which are the same than the ones to be used in the first LST of CTA.

4.2 The SRD device

The Step Recovery Diode (SRD) is essentially a pin diode with a very thin i layer, and with a very abrupt n and p doping distribution (p+-i-n+). It was introduced by Boff, Moll and Shen [1], [2]. The special feature of this device is its very steep turn off, which gives it the ability to generate very sharp pulses containing many harmonics. For that reason it is employed in a wide variety of applications: harmonic generation [3], frequency multipliers [4], sampling [5], sharpening and pulse generation [6][7], etc…

Of special interest are the very common topologies for designing pulse generators which combines the SRD and delay lines [8], [9]. However, a wide range of other structures can be used, as for example the design carried out of a low jitter (5 ps) pulser presented in [10], whose width can be modified from 1 to 10 ns by controlling the SRD forward current. For UWB applications where low frequency components are not desired, in particular DC, the monocycle pulse generators can be used [11], [12]. Finally it is remarkable the pulse-sharpening circuit described in [13] which uses a diffused SRD for increasing its breakdown voltage, very interesting when high voltage values are intended to be use.

The SRD physics and dynamic behavior has been deeply investigated and there is a wide variety of documentation about it, from the most basic analysis [14] to detailed studies as the carried out by Agilent in its application note 918 [15], which includes pulse generators examples. Other noteworthy literatures are the accurate dynamic model of the SRD presented in [16], the study of the transient behavior under resistive (step recovery) and inductive (ramp recovery) switching conditions performed in [17], or the analysis of the reverse recovery mechanism using the Laplace transform in combination with the Greens's function technique developed in [18]. Also remarkable is the rigorous research of the SRD intrinsic parameters and its influence on the device behavior, carried out by M.J. Chudobiak [19], and focused on designing high voltage SRDs. Finally, an interesting brief guide for selecting SRDs can be found in [20].

During forward conduction the SRD stores charge in the i-layer, which is accumulated close to the junction as the intrinsic region is quite narrow. When it is reverse biased, the SRD has first to remove all the stored charge before it can follow the input voltage. While the charge is being extracted the SRD presents very low impedance and its terminal voltages remains almost constant. Once nearly all the storage charge has been depleted, the SRD

suddenly changes to its high reverse impedance state and consequently its terminals switch to the negative voltage input. This transition happens extremely fast.

In the Figure 4.2 the electric field distribution during the reverse transition is shown. As the mobile carriers (electrons and holes) are being depleted from the edges of the i-layer, a voltage develops at the two boundaries as a consequence of the generation of space charge regions. During the middle intervals of the transition there is still high density of carriers in the center part of the intrinsic region so the electric field is zero. As the center loses its charge the space charge regions get wider and the voltage increases.

Once the intrinsic layer has been almost exhausted of carriers the "punch through" situation takes place. In that moment the two space charge regions overlap and the electric field "snaps" taking up the entire intrinsic layer. The remaining carriers are then swiftly depleted and the voltage across the diode switches to its final value.

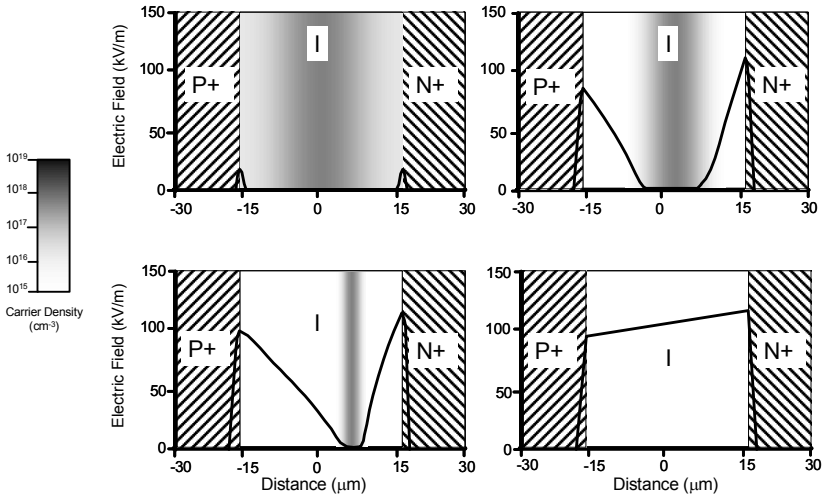


Figure 4.2 SRD electric field distribution during a transit from a forward bias to a reverse one

The ability for storing the injected electrons and holes comes from a long enough minority carrier lifetime that guarantees that they do not immediately recombine, due to the intrinsic layer. The stored charge during forward biasing in the SRD is determined by the continuity equation [21],

$$i(t) = \frac{dQ(t)}{dt} + \frac{Q(t)}{\tau} \tag{4.1}$$

where τ is the minority carrier lifetime, i(t) is the diode current and Q the stored charge.

Assuming a constant forward current I_F, the solution for the stored charge yields,

$$Q_F = I_F \tau \left(1 - e^{-t_F/\tau}\right) \tag{4.2}$$

where t_F is the time in forward conduction.

If $I_F \gg \tau$,

$$Q_F \cong I_F \tau \tag{4.3}$$

τ is not usually constant and depends on level of stored charge.

Following, the time required for extracting all the stored charge Q_F (called storage time) by applying a reverse current I_R is:

$$t_s = \tau ln\left(1 + \frac{Q_F}{I_R \tau}\right) = \tau ln\left(1 + \frac{I_F\left(1 - e^{-t_F/\tau}\right)}{I_R}\right) \tag{4.4}$$

Similarly if $I_F \gg \tau$,

$$t_s = \tau ln\left(1 + \frac{I_F}{I_R}\right) \tag{4.5}$$

As can be observed, higher values of the charge result in a longer storage time to extract it, as it results obvious.

When working with step recovery diode there is an effect that is present in the design, the voltage spike. This is produced by the fast change of the diode current through the package inductance, and comes determined by,

$$V_L(max) = L_p\left(\frac{di}{dt}\right) \tag{4.6}$$

Nowadays, manufacturers try to make the package inductance as small as possible, but when working with very rapid transitions it is a parameter to take into account.

Finally, another characteristic of the SRD is its variable impedance. During forward conduction it is about 1-20 Ω and in reverse is 50-500 Ω.

For the behavior above presented, the step recovery diode is also called "Snap-off" diode, "charge storage" diode or "memory varactor".

4.3 Baseline design

Figure 4.3 shows the schematic of the pulse generator based on a Step Recovery Diode (SRD) developed. It is composed by a low bandwidth pulse generator and a pulse shortener. The slow transition times of the initial pulse is converted into a faster transition time pulse at the output of the shortener stage.

The low bandwidth pulse generator is based on a Schmitt-Trigger inverter with asymmetric feedback. The charge and discharge of the input capacitor controls the input and output states of the inverter. When the capacitor is discharged, the logic output of the

inverter is 1. Consequently, there is a current flow towards the capacitor through resistor R2 with a R2·C1 time constant. The diode is in off state and impedes the current across R1. Once the voltage across the capacitor reaches the positive threshold, the inverter changes to the logic status 0. Then the capacitor starts to discharge through the parallel of R1 and R2 (the diode is now on) with a time constant of (R1//R2)·C1. This process is cyclically repeated producing the low bandwidth pulses. The repetition frequency and the pulse width are adjusted by means of R1 and R2. A further analysis of the behavior of this pulse generator can be found in Appendix C.

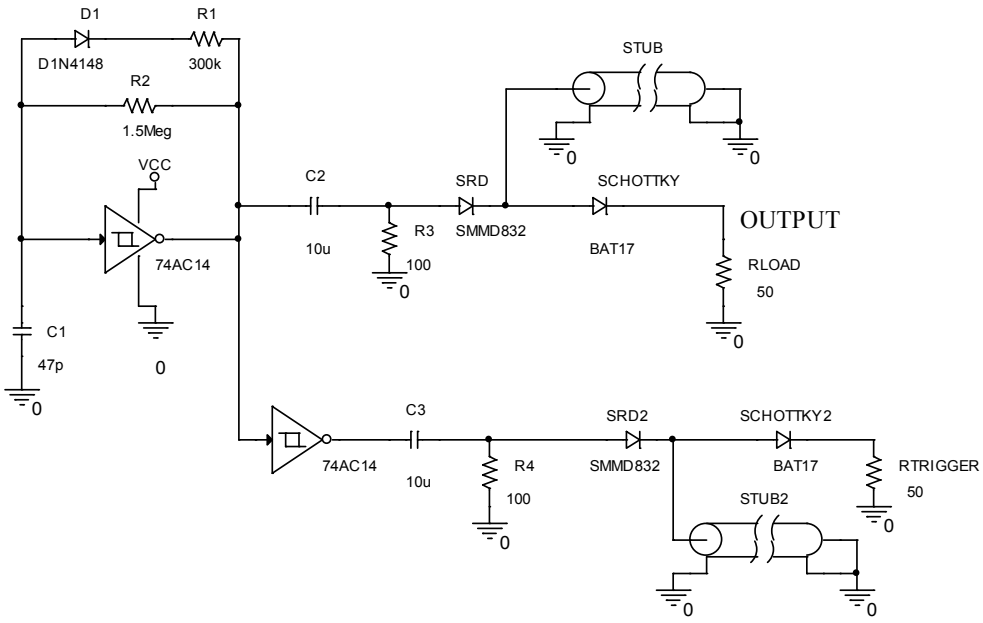


Figure 4.3 Pulse generator schematic

The pulse shortener is mainly composed by a SRD and a short-circuited stub. A high value capacitor is placed before this stage in order to filter the DC signal. Then the input voltages to the SRD are controlled by means of the duty cycle of the low band pulse generator. This adjustment is of great importance because of the output pulse depends on the charge and discharge times of the diode and consequently on the minimum and maximum voltages applied to the SRD. Input voltage levels from around -3 to 1 V have been fixed.

A simulation of the current and voltage values across the SRD, the stub and the load is shown in Figure 4.4. During the positive part of the pulse the SRD is under forward conduction and the minority carriers are stored into the i-layer. The stub is short-circuited so all the current goes through it. There is no current across the load and therefore the output voltage is zero. Next the SRD is reverse biased and starts to discharge. During the storage time the diode remains in conduction in a low impedance state, and its terminals cannot follow yet the input voltage. Thus, the voltage across the SRD stays almost constant. At high frequencies the length of the stub is not negligible [22] and there is a delay between the

current at the SRD and the current at the stub. This delay causes the current to flow from the load and consequently a negative output pulse. In the current simulation of Figure 4.4 this behavior can be observed, where the sum of the currents flowing into the node composed by the SRD, the stub and the load is equal to the sum of the currents flowing out of that node, so Kirchhoff's current law is preserved.

Once almost all the charge has been extracted, the SRD changes suddenly to high impedance (punch through). The voltage across the diode varies rapidly creating a sharp and fast transition edge. The signal sunk in the short-circuited stub is reflected with opposite polarity and cancels the input signal when returned after the delay time. The width of the output pulse is then determined by the length of the stub.

The negative pulse observed during storage stage of the transition is canceled by means of placing a Schottky diode (BAT17), which involves a loss in the amplitude of the output pulse of about 200 mV.

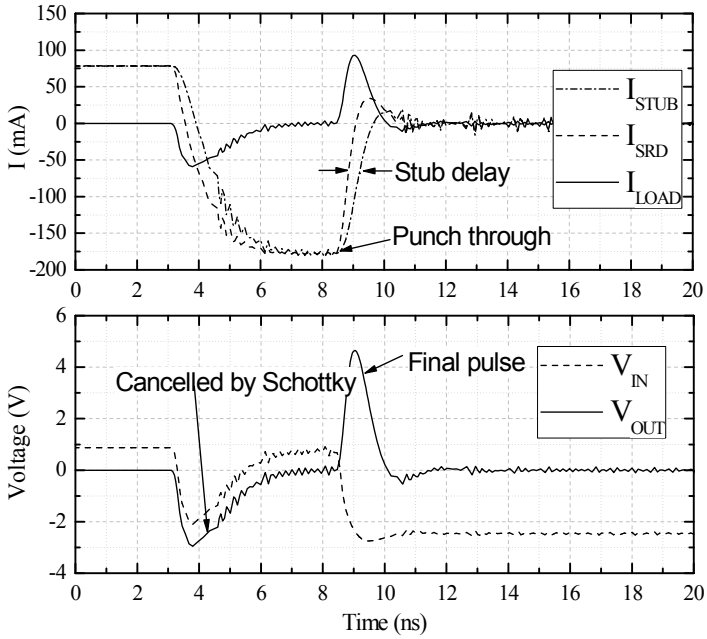


Figure 4.4 Pulse generator shaping. Top: Current in the diode (I_{SRD}), stub (I_{STUB}) and load (I_{LOAD}). Bottom: Voltages at the input (V_{IN}) and output (V_{OUT}) of the SRD. The signals were simulated by removing the Schottky diode from the schematics of Figure 4.3.

The model of step recovery diode employed in the pulse generator here presented is the SMMD832 from Aeroflex-Metelic [23], whose main characteristics are a 12 ns carrier lifetime, 70 ps transition time and 0.6 pF junction capacitance. An accurate model obtained from the manufacture web has been introduced in ORCAD simulations.

The stub implemented in the design is a conductor-backed coplanar waveguide (CBCPW), which transmits quasi-TEM modes. The software ORCAD used to perform the simulation does not have available this kind of transmission lines, but instead it has coaxial

ones that transmit pure TEM modes. In order to perform an accurate simulation, the associated parameters to the coplanar waveguide are calculated by means of the software APLAC and next introduced in the equivalent coaxial transmission line of the ORCAD simulation. The parameters that define the transmission line are the effective permittivity and characteristic impedance.

The geometry and characteristics of the stub play a decisive role in the output pulse shape. Figure 4.5 shows dependence of the output pulse with the stub length for a fixed value of the impedance. On the other hand, the influence of the stub impedance for a fixed value of its length is also represented.

The characteristics of the stub carried out are the following: 112 mm length, 1 mm width and 0,5 mm gap to ground. It has been fabricated on a FR4 glass epoxy substrate, with εr=4.5, 1.6 mm double sided board thickness and 36 µm copper thickness.

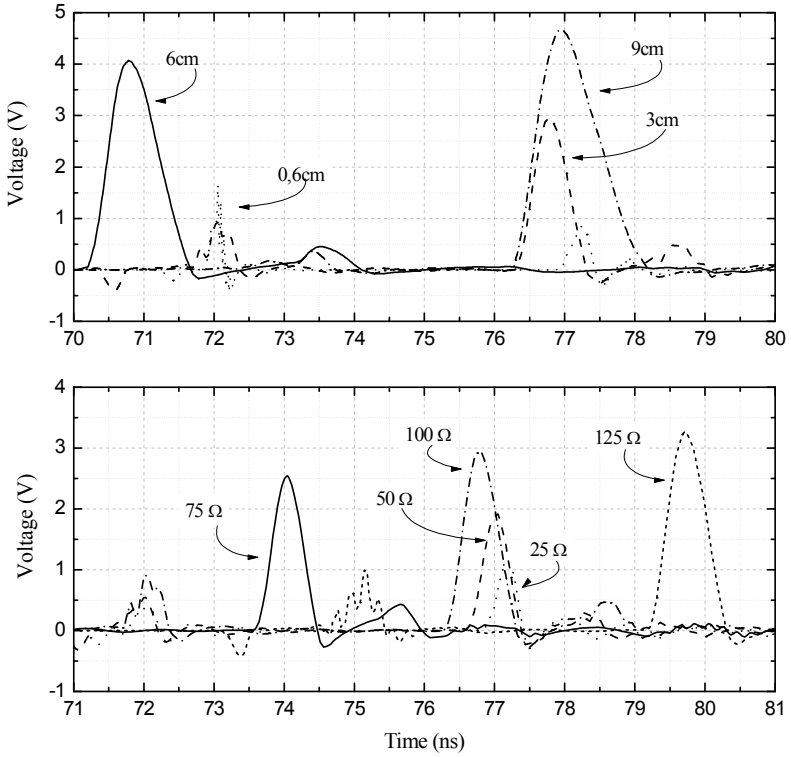


Figure 4.5 Effect of the stub length for a fixed impedance of 100 Ohm (top) and stub impedance (bottom) for a fixed length of 6 cm on the performance of the generator.

A pulse of more than 4 V of amplitude and 1.32 ns of width has been achieved (Figure 4.6). Also, a very high concordance between simulation and experiment has been obtained. It is important to remark that with this design it is possible to get much narrower pulses, and widths of around 300 ps have been measured in different prototypes carried out. Nevertheless, the requirements were a pulse generator of the characteristics here presented.

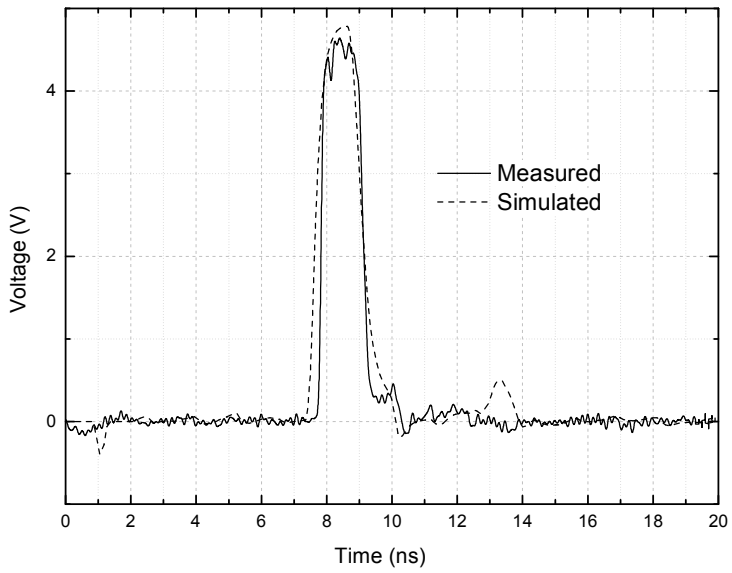


Figure 4.6 Comparison between the simulated and measured pulse shape

Finally, jitter measurements have been carried out. As it was described in detail in Chapter 3, the jitter is a very useful figure of merit of pulse generators. Figure 4.7 (top) shows the histogram of the pulse width, obtaining a pulse width jitter of 6.32 ps and a mean value of 1.324 ns. No deterministic jitter is observed, as there is just one Gaussian distribution and no more peaks are appreciated. For the repetition frequency, a standard deviation of 23.5 ns has been measured and a mean value of 45.42 s (Figure 4.7 bottom).

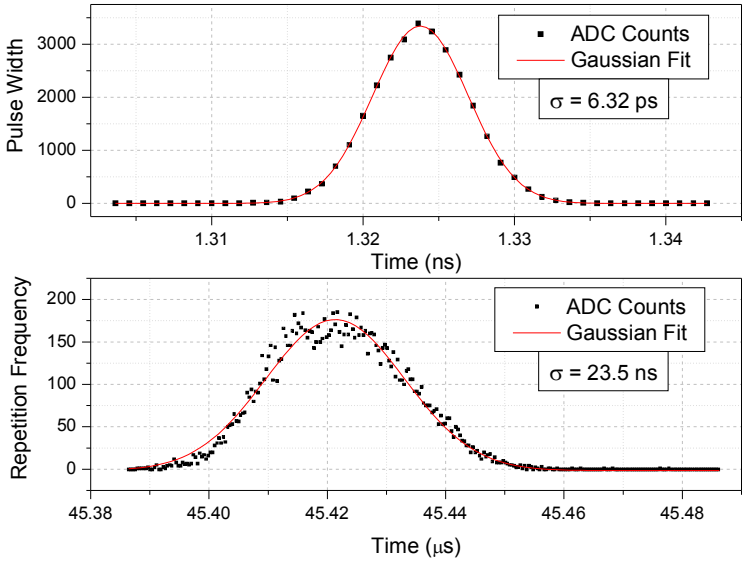


Figure 4.7 Top: pulse width histogram. Bottom: repetition frequency histogram

Figure 4.8 shows the pulser once implemented. It can be noticed that another output has been taken, this time from the non-inverted output of the Schmitt-Trigger inverter, which can be employed as trigger signal.

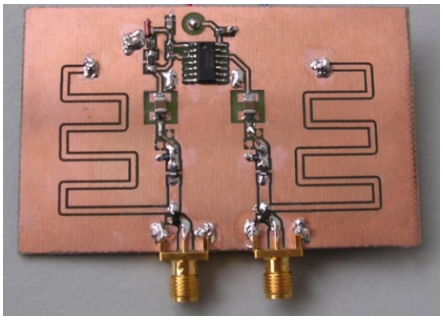


Figure 4.8 First prototype of the SRD pulse generator with a trigger function

4.4 Fanout scheme

The output of the pulse generator is split next in four channels. The design of this stage is crucial in order to achieve a good performance, so it has to accomplish with strict demanding features: a) it has to be matched to avoid pulse ringing, b) the four outputs must have the same length, and c) it must not produce any distortion in the wave shape. A resistive power divider has been chosen for that purpose (Figure 4.9) due to its excellent broadband response and simplicity at the expense of a higher loss compared with other possibilities as for example reactive dividers.

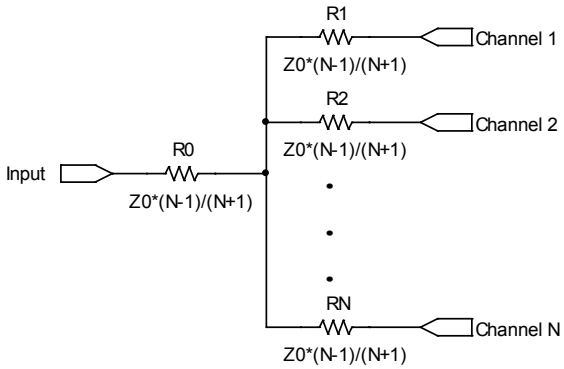


Figure 4.9 N-way resistive power divider

The values of the resistances that minimize power loss are determined by following equation [24].

$$R = Z_0 \frac{N-1}{N+1} \tag{4.7}$$

where N is the number of outputs and Z_0 is the characteristic impedance of the system, that in this case is 50 ohms. The transferred power ratio at each output is $(1/N)^2$ and therefore the insertion loss is $10log_{10}(1/N)^2$. Then for a 4-way divisor it yields, $R = 30\ \Omega$; $P_{loss} = -12.04\ dB$.

In order to obtain the same electrical length in all the channels, a vertical input and horizontal output symmetric design has been carried out. The input resistor has been placed into the hole performed to connect the bottom and top board sides. Figure 4.10 shows the first version that was developed and successfully tested.

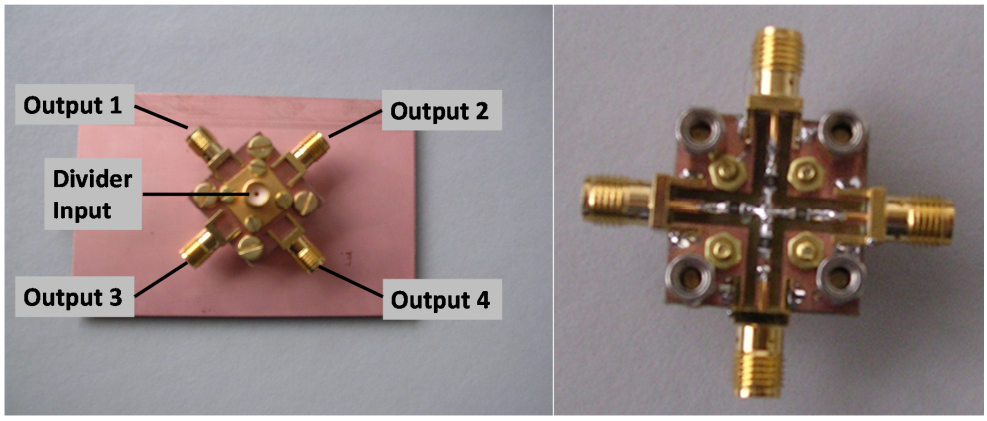


Figure 4.10 Fanout board

The tests were made with input pulses of 4 ns width, 3 V amplitude and 2.5 ns rising and falling times. A 240 MHz oscilloscope (Tektronix AFG3252), with a 50 ohm input impedance was used to take the measurements. All the outputs must be connected to matched loads in order to prevent spurious reflections. The measured pulses are shown in Figure 4.11.

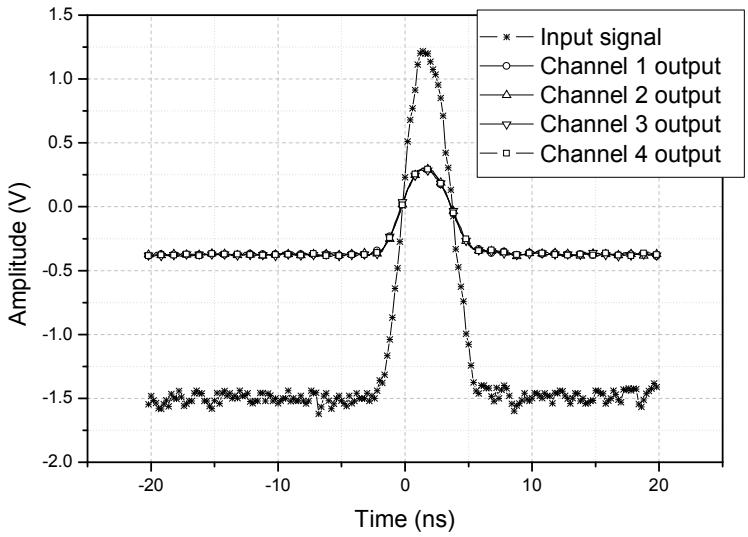


Figure 4.11 Comparison between input and outputs of the 4-way divisor

From this figure it is observed that the dissipative power divisor does not introduce any perceptible distortion. In addition, the four outputs are identical. The amplitudes of the input and output pulses are 2.75 and 0.7 V, respectively. The slight deviation with respect to the 3 V amplitude configured in the function generator used as signal source is attributed to the connectors and wires. Consequently, the power loss at each channel yields,

$$P_{loss} = 20log\frac{V_{out}}{V_{in}} = 20log\frac{0.7}{2.75} = -11.88\ dB$$

There are practically no discrepancies between the theoretical 12 loss and the measured value.

4.5 Pulse amplification

The fanout preserves the pulse integrity at the expense of significant power losses, as was shown in previous Section. So it was necessary to amplify the output pulses. A 4-channel amplification board was designed with this purpose. This circuit also isolates the pulse generator from possible reflections produced at the load, thus avoiding distortion. The amplifiers feature a S_{12} parameter very close to zero, blocking the transmission in the opposite direction. This is important in applications where the load present impedance changes, as lasers or LEDs.

In order to achieve a good output pulse shape, the amplifier has to be carefully chosen. Bandwidth, gain, linearity, dynamic range and noise figure are critical parameters to take into account in the selection. The input pulse has a width of 1.32 ns so it is required a bandwidth of at least from DC to 800 MHz, where the main lobe of the signal is contained.

The gain block model 7489Z [25] from RFMD was chosen. This is a high performance MMIC (Microwave Monolithic Integrated Circuit) amplifier based on the SiGe HBT technology, with an operation range from DC to 3000 MHz. In particular, at 850 MHz it features a gain of 21.5 dB, a third-order intercept point of 35.5 dBm, a 1 dB compression point of 22.4 dBm and a noise figure of 2.8 dB. Finally, its 3 dB bandwidth is more than 1 GHz.

The schematics of each one of the four channels is shown in Figure 4.12. The amplification board is composed by two amplifiers in cascade per channel. It was made in this way because the 7489Z is an inverter amplifier.

On the other hand two attenuators have been used. The first one with a value of 16 dB has been inserted at the input of the power divider in order to prevent the saturation of the first amplifier. The second attenuator of 6 dB has been placed between the two amplifiers to avoid the saturation of the second amplifier. Both of them also minimize pulse

ringing and distortion. Additionally a feedback resistor in the second amplifier modifies its operation point reducing its gain and allowing consequently a higher power at its input without entering into saturation.

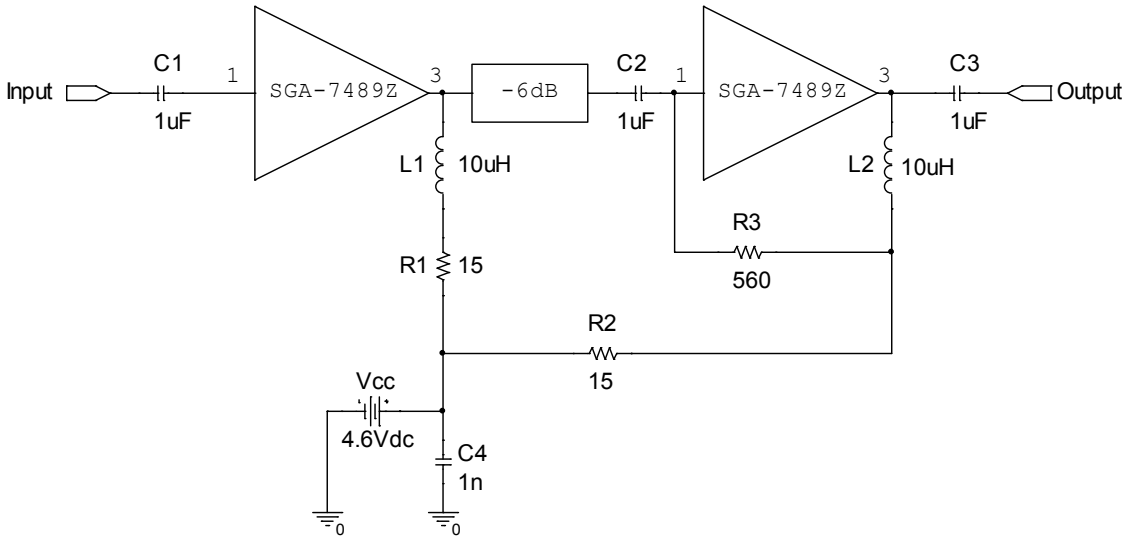


Figure 4.12 Schematic of each channel of the amplification stage

Four independent biasing nets have been designed in order to avoid signal transfer among the channels via the same voltage source. This part of the circuit has to be capable for filtering the high frequencies corresponding to the input pulse and any undesirable signal. Also, it has to be able to supply relatively high currents (about 150 mA). Special attention must be taken on the resonance frequency of the selected components. On the other hand, 1 uF capacitors are placed at the input and output of each amplifier for DC blocking purposes. Figure 4.13 shows the first prototype that was successfully implemented.

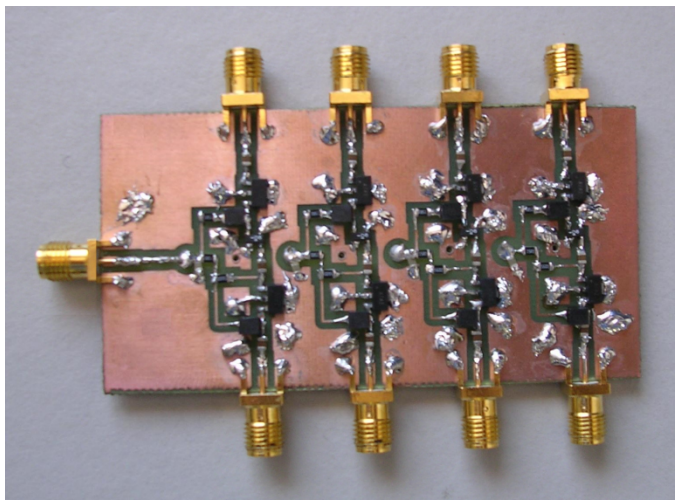


Figure 4.13 Amplification board

4.6 Prototype for MAGIC

4.6.1 VCSEL biasing boards

In this section the VCSELs biasing boards are developed. Each one of the VCSEL requires a current bias of 3 mA, so a stable DC current source is carried out. The design here presented is based on an improve version of the Howland current source [26], which is detailed by Rafiei-Naeini and McCann in [27], and was proposed for the MAGIC II telescope camera.

Figure 4.14 shows the implemented current source circuit, based on the low noise operational amplifier OP27 from Analog Devices [28]. This device features a noise of just $3.5\ nV/\sqrt{Hz}$ at 10 Hz, a 1/f noise corner frequency of 2.7 Hz and a low drift of 0.2 V/°C. Low noise usually involves a lesser output current handling, but it is a priority facet in this design for minimizing the noise introduced to the VCSELs. In this case a single OP27 is not capable of driving the four VCSELs, so two bias networks have been carried out (an OPAMP to every VCSELs). The current supplied to the VCSELs can be adjusted by means of the control voltage,

$$I_{VCSEL} = \frac{V_{Control}}{2R_{Bias}} \tag{4.8}$$

where the factor 2 in the denominator takes into account that each OPAMP feeds two VCSEL. Additionally an inductive filter per VCSEL has been added in order to avoid the pass of AC current through the bias network. A resistance in parallel to the higher value inductor has been placed in order to reduce its resonant quality factor and consequently avoid from signal distortion. Some other filter configurations have been tested but the best behavior has been achieved with the one here presented. In particular, a capacitor between the two inductances to ground was placed trying to achieve a more robust filter, but on the contrary resonance problems appeared. Finally, for the insertion of the VCSELs pin holders have been placed in the board to avoid the need for soldering them.

The OPAMP has been single biased at 10 V for reducing the number and the level of voltage sources, even if the recommended supply voltage is of about $\pm 15\ V_{DC}$. Successful results have been obtained in the laboratory tests achieving the 3 mA required for each VCSEL at a voltage control ($V_{Control}$) of 3.4 V, as predicted by the simulation (Figure 4.14). The VCSEL has been simulated as a 75 ohms resistor.

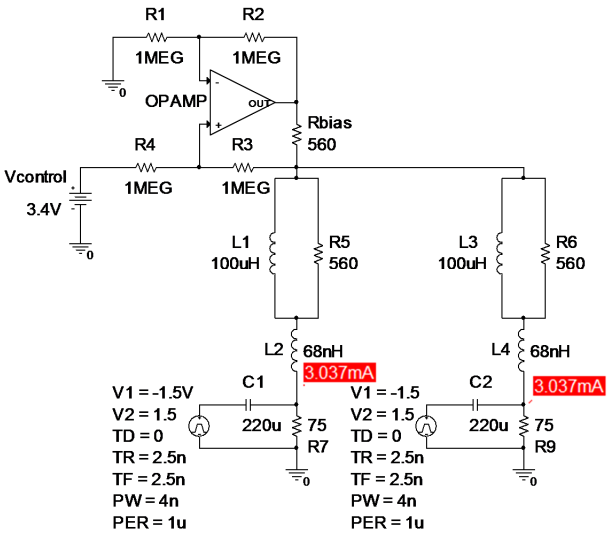


Figure 4.14 VCSELs bias board schematic

In order to evaluate the signal integrity and the crosstalk between channels two measurements have been carried out. First, a pulse has been sent to the RF input of the boards and the signal at the VCSELs' holders has been measured. Doing so it is analyzed the quality of the signal that the lasers will receive. The characteristics of the pulse are the following: 3 V of amplitude, zero offset (that is, from -1.5 to 1.5 V), 4 ns width and 2.5 ns for both transition times (the narrowest pulses achievable with the function generator available at the laboratory). These measurements have been carried out without biasing the boards and without placing the lasers, as the interest of the tests is to verify that the passive filter and the layout do not introduce any distortion. The results obtained are shown in the left graphic of Figure 4.15.

Second, the effect caused by signals received in other channels is analyzed. For that purpose a similar pulse as the used in the previous test is introduced at port 1 and another one but with different frequency is introduced at port 2. The analysis has been carried out for the frequencies of 10 MHz and 120 MHz. Results are shown in the right graphic of Figure 4.15. Other tests are also possible. For example, if the instrumentation required is available, to perform a frequency sweep of the waveform transmitted results a good option for analyzing cross-talk.

From the results obtained it can be concluded that the integrity of the signal is completely preserved as the signal at the lasers holders keeps the shape of the input pulse (left graphic). There exists a small attenuation due to the losses produced in the connection wires: the data acquisition of the pulse has been made by connecting the function generator directly to the oscilloscope, while the measurements of the signals at the holders have been taken by connecting the function generator to the board and then the board to the oscilloscope.

Regarding to the graphic of the right, it can be remarked that there is a bit of distortion in the signal measured. The level of distortion is less than the 20% of the signal applied to the other port, so it can be concluded that the filters feature a good behavior. It is remarkable that in other designs tested the level of distortion was greater than the 50% of the signal.

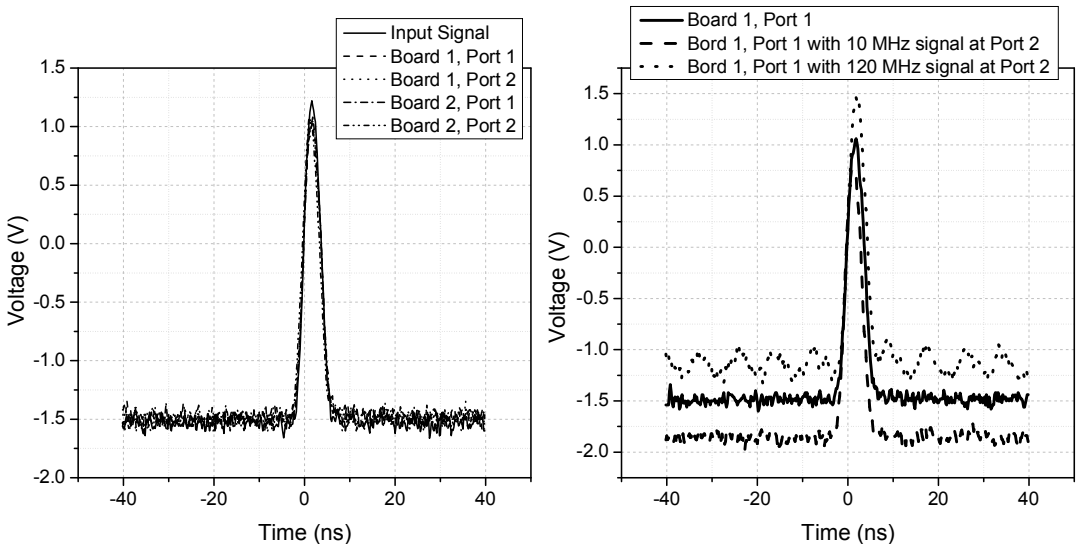


Figure 4.15 Right: signal integrity test, and left: crosstalk test

A change in the DC level of the signal can also be observed. It is due to the direct current of the signal inserted at the other port. In real conditions the RF signal comes from the amplification stage, which has an output capacitor, so the offset in DC level will not be present. Finally, Figure 4.16 shows the VCSELs bias boards once implemented.

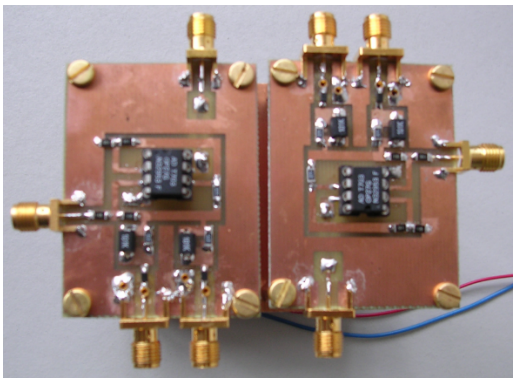


Figure 4.16 VCSELs bias boards

4.6.2 DC Regulation

A DC regulation board has been carried out in order to supply all the system by means of a single power source. This circuit will bias the pulse generator, the amplification and the VCSEL boards. One of the higher problems encountered in DC regulation is the 1/f noise. Switching power sources are very commonly used nowadays due to its high efficiency, low size and low cost. Nevertheless, they introduce high noise levels. On the other hand three-terminal resistive regulators introduce less noise at the expense of a greater consumption. As power consumption is not a critical factor in this design but noise performance is, resistive voltage regulators were selected. The power requirements of the system boards are shown in Table 4.1.

Pulse generator board	Amplification board	VCSEL biasing boards
$V_{CC} = 5.5\ V$ $I_{CC} = 31\ mA$	$V_{CC} = 4.6\ V$ $I_{CC} = 610\ mA$	$V_{CC} = 10\ V$ $V_{Control} = 3.4\ V$

Table 4.1 Voltage requirements

For this design the regulator LM317 has been used. In particular four regulators have been necessary, one for each voltage required. The input voltage to the board has been selected at 12 V for two reasons: it is compatible with all the demanded voltages (the higher value needed is 10 V) and it is a standard value in supply voltages. Figure 4.17 shows the schematic of the global bias board. By means of the potentiometer the output voltage is adjusted for each channel. If a poor stability voltage source is used, it is convenient to add a capacitor of about 0.1 F between the input and ground. Additionally, decoupling capacitors have been placed at all the power supply inputs of the boards that compose the prototype in order to prevent excessive voltage ripples and noise (not shown in the schematics).

Special attention needs to be taken for the regulator used to supply the amplification board. This device has a T0-220 packaging and supports a 1,5A maximum current. However, due to the demand of current (about 600 mA) and the high voltage drop across it (from 12 V to the 4.6 V required), the regulator produces an excessive quantity of heat. Even if it includes an internal thermal overload protection that prevents the regulator from damage, the result would be an improper working, as it immediately reduces or cuts the output current.

For that reason the following improvements were made: 1) to place a heat sink on the regulator (with thermal paste between the surface of both), and 2) to place two resistors in parallel for reducing the input voltage to the regulator and consequently the power dissipation - there is a minor voltage drop across the regulator. The resistances placed have been of 10 ohms and 2 watts each one, achieving a total power loss of about 1.8 watts and a voltage drop of 3 V. Figure 4.18 shows this board implemented.

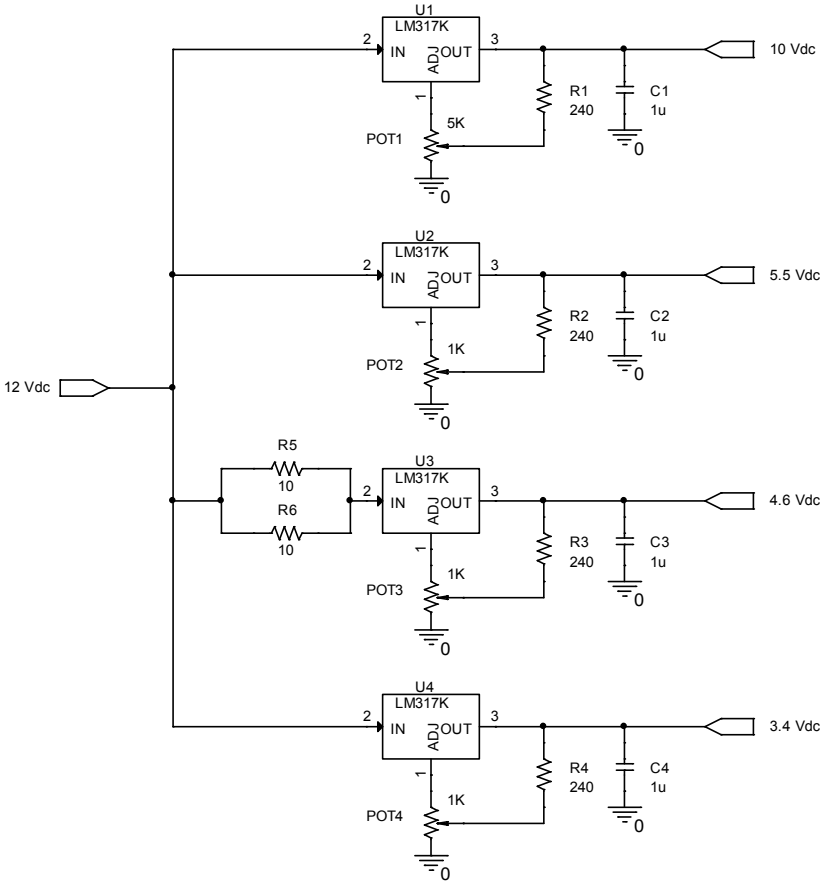


Figure 4.17 DC regulation board schematic

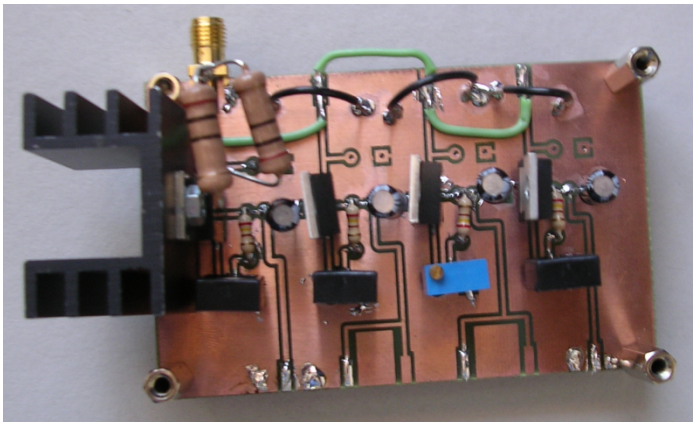


Figure 4.18 Detail of DC regulation part

4.6.3 Experimental Outcomes

The full system once assembled is shown in Figure 4.19. The modular design carried out have permitted an independent design and optimization of each board. Also, it makes easier the substitution of one part of the circuit in case of future improvements. On the other hand, it is

the best alternative for achieving the same electrical length in all the channels. All the boards used in the design are FR4 laminates with 1.57 mm substrate thickness. A summary of the components used for the SRD pulse generator can be found in Appendix D.

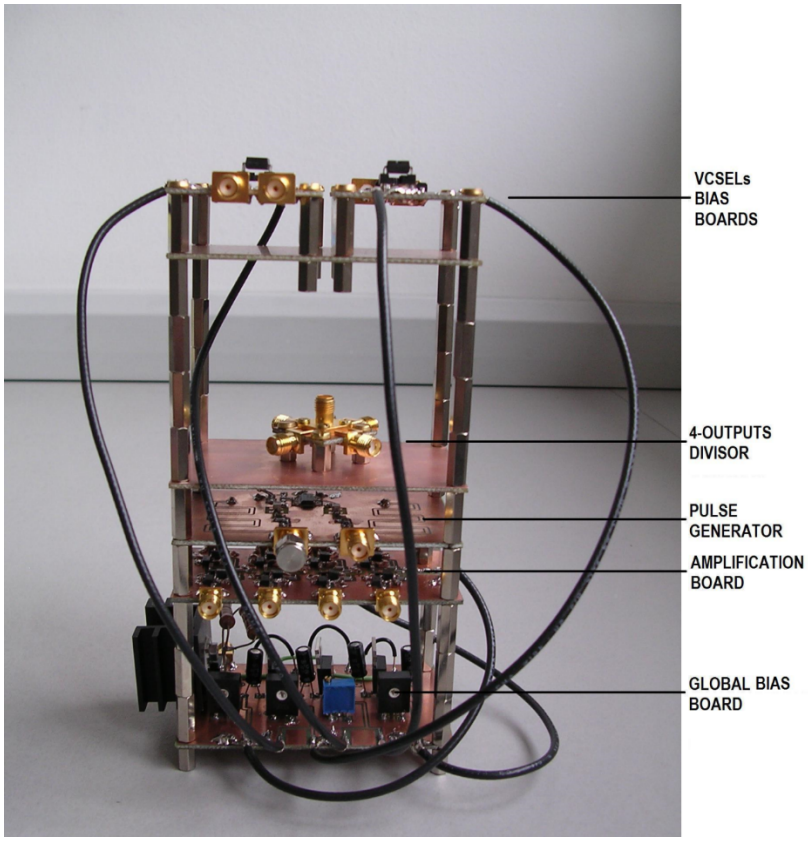


Figure 4.19 Full System

The signal throughout the entire system was been measured. In Figure 4.20 (top) the output of the pulse generator is represented. A pulse with more than 4.5 V of amplitude and a width of 1.3 ns has been achieved. This is a very good result due to the complication in obtaining a pulse of such characteristics.

Figure 4.20 (bottom) shows the same output but placing a 550 MHz filter before the oscilloscope. This test has been done in order to simulate the result obtained if a 500 MHz bandwidth would have been used to perform the measurement, very usual in most laboratories. This demonstrates the need of having available a wideband oscilloscope for the accurate measure of this kind of pulses. The oscilloscope used had a bandwidth of 6 GHz.

The second output of the pulser, connected to the non-inverting port of the 74AC14, has been also measured (Figure 4.21). The pulse obtained has a width of about 990 ps – 1 ns and 2.8 V of amplitude. The differences on the waveform come for the fact that the system design was optimized for the other output. This output can be used as trigger signal.

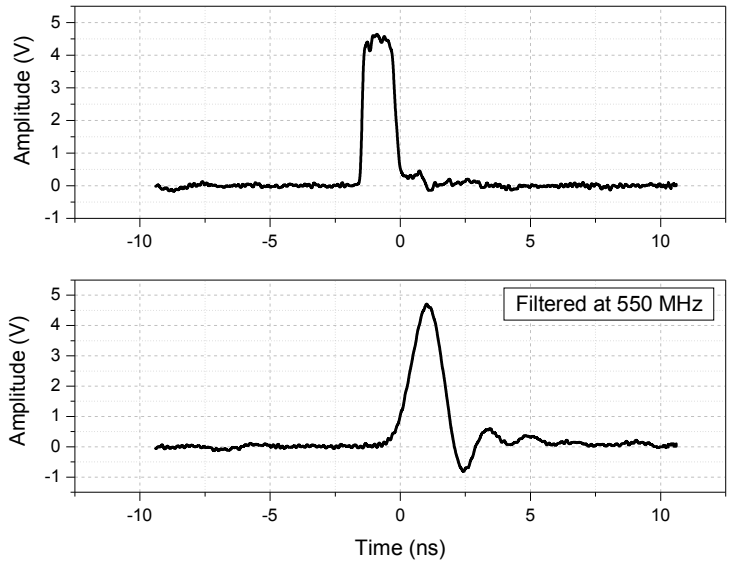


Figure 4.20 Top: pulse generator output. Bottom: pulse generator output filtered at 550 MHz

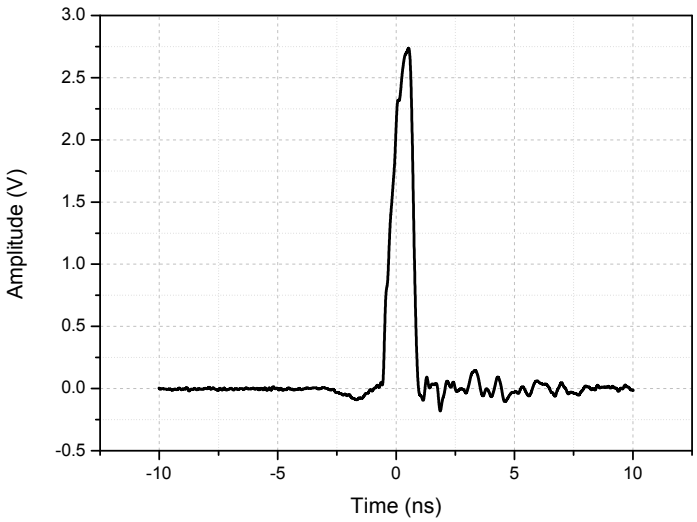


Figure 4.21 Second output pulse generator

The pulse is next connected to the 4-way divisor. Due to the level of signal even at the output of the divisor is too high, it saturates the first amplifier of each channel of the amplification board. For that reason a 16 dB attenuator has to be placed between the output of the pulse generator and the input of the 4-way divider. The 16 dB attenuated output pulse signal of the generator is shown in Figure 4.22 (top), with a value of the amplitude of less than 0.8 V. The four signals after going through the power divider are shown in Figure 4.22 (bottom). All of them are identical and any delay is noticeable among them.

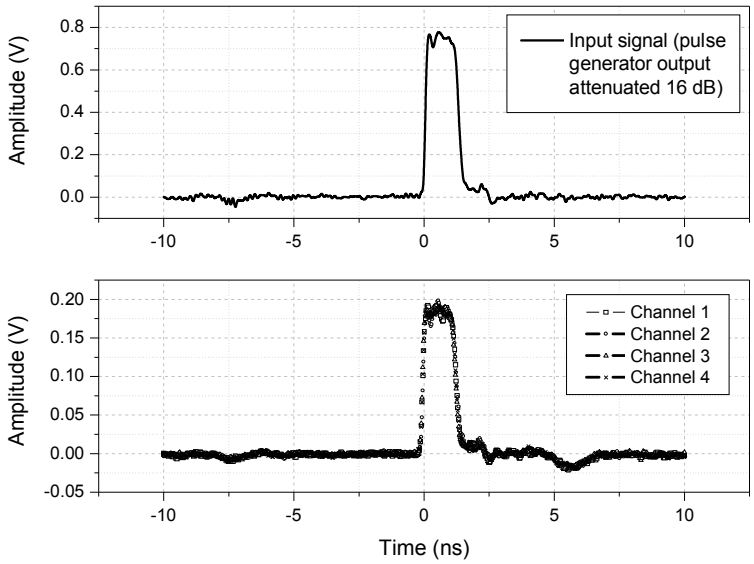


Figure 4.22 Top: pulse generator output signal 16 dB attenuated. Bottom: outputs of the 4-channel divisor

Finally the four signals are independently amplified (Figure 4.23). Four similar pulses of the required 4 V amplitude and 1.3 ns width have been achieved. It is noticeable to remark that the pulse width has been kept throughout all the stages of the design, so the system does not widen the pulses. As well, all the channels are received in phase, issue very important in the design, so there is a perfect symmetry among all channels.

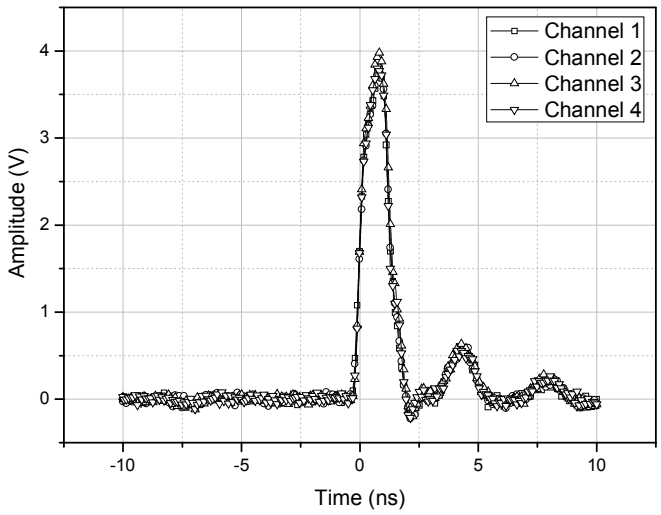


Figure 4.23 Amplification board output pulses

4.7 Prototypes for readout boards (MAGIC Upgrade and CTA)

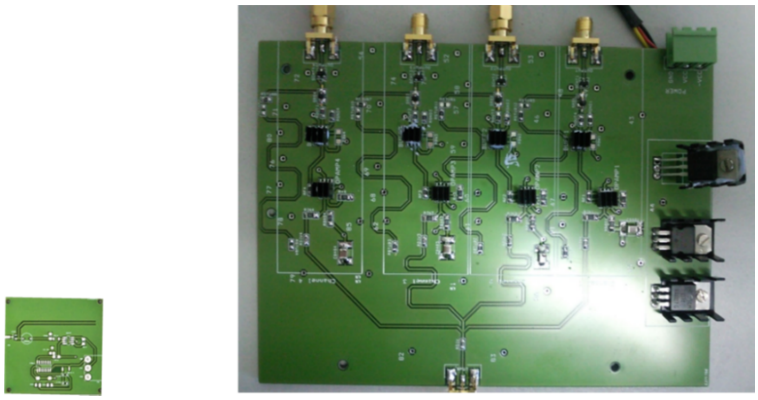
In the years 2011-2012 the MAGIC telescopes underwent an upgrade whose major technical novelty was the change of the readout board to one based on the last version of the DOMINO chip, the DRS4. This was also the chip used in the first LST of CTA. After this upgrade the readout electronics, divided in two main parts: the receiver boards and the digitization electronics, could both be controlled by the same VME-based communication network.

The new MAGIC readout performs the sampling of the signals at a rate of 2 Gsamples/s. It is cost effective, has a linear behavior over a large dynamic range (from less than 1 photoelectron (phe) to about 600 phe), less than 1% dead time, low noise, and negligible channel-to channel cross-talk [29], [30] (Sitarek et al. 2013; Bitossi et al. 2014). This allowed maintaining the performance of the initial readout based on MUX-FADCs while increasing the charge resolution, reducing cost and saving space. Reducing the space occupied by the readout electronics was very important. In fact, the electronics room hosting the trigger and readout of the two telescopes was not large enough to host a readout of more than 2000 channels in a previous configuration. Through the upgrade to a more compact DRS4 system only 6 racks were needed for the trigger and readout system of the two telescopes. A modular system of 13 boards with 96 channels each was implemented to accomplish this.

Thus, the four channel pulse generator design presented in the previous section provided a basis for the development of a 96 channel pulser prototype, which was carried out by the UCM-ELEC group. Since the boards had to be outsourced to an external company, the substrate differs from the FR4 one used in the previous prototype, which was fabricated with the photolithography available at the Microwave laboratory of the UCM. The 96 channel pulse generator was successfully used for testing the readout boards of the MAGIC upgrade. These tests were performed at the INFN (Istituto Nazionale di Fisica Nucleare) with the support of the UCM-ELEC group. The prototype was also proposed for testing the CTA readout boards (named Dragon boards) which are based on the same DRS4 chip.

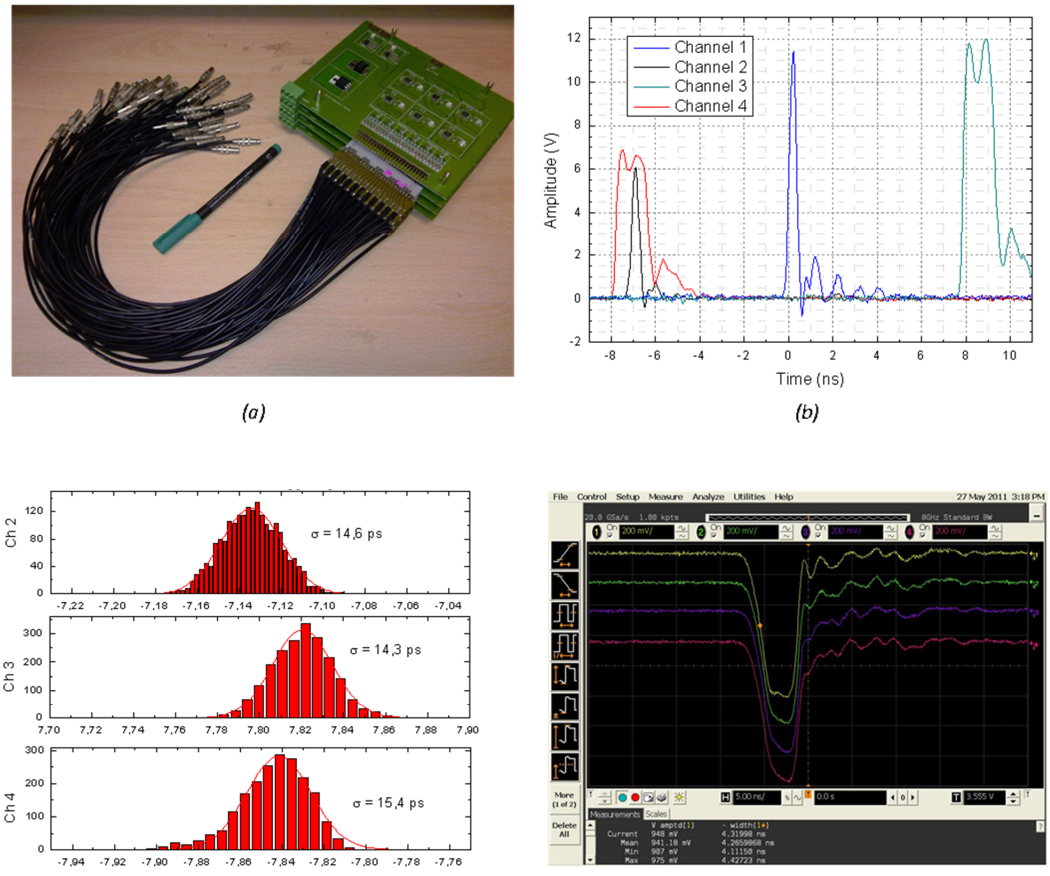
The new substrate demonstrated to feature better characteristics in terms of losses and reliability. A single channel pulse shaper was first fabricated with the new substrate in order to optimize the layout for the pulse shortening stage, which needs a short circuit stub. The first prototype is shown in Figure 4.24a. Then a 4 channel prototype was fabricated, which is shown in Figure 4.24b. The 96 channel version was implemented in four boards, each one containing six pulse shaping circuits with the outputs connected to six fanout circuits. Each fanout divided a single pulse channel into four, using the same scheme that was described in Section 4.4. Figure 4.25a shows the final prototype. The main measurements summarizing its performance are shown in Figures 4.25b (pulse shapes), 4.25c (jitter), 4.25d (S11 of pulse fanout) and 4.25e (S21 of pulse fanout). The pulse shapes shown in 4.25b were obtained by playing with different resistors in the pulse shaping circuit. As it can be seeing, voltage peaks of up to 12 V and pulse widths as short as 370 ps could be obtained at the

outputs of the first fanout. Using the configuration of channel 4 for the 96 channel prototype the voltage peaks at the final stage were of the order of 980 mV.



(a) *(b)*

Figure 4.24 Pulse shaping circuit with new substrate. (a): single channel for layout optimization, (b) four channel prototype.



(a) *(b)*

(c) *(d)*

Figure 4.25 96 channel prototype. (a): photograph, (b): pulse shapes that can be obtained by changing the resistor of the pulse shaping circuit, (c): jitter as measured in the four channel board (triggering on Ch1) and (d): pulse shapes at the outputs of the fanout (channel 4).

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Chapter 5. Signal on Transition pulse generator

5.1 Introduction

In this chapter a new type of low width pulse generator is developed, offering some benefits regarding the SRD pulse generator. Based on the Patents US 6433720 [1] and US 6642878 [2] created by Furaxa, the main body of the design is mainly composed by 4 MOSFET transistors whose accurate switching generates the output pulse.

One limitation that can be found with the previous SRD design is that the output pulse width is fixed to a particular value, as it determined by the length of the stub. Depending on the application, it can be really helpful to be able to vary the pulses width. Sometimes it is necessary to perform an accurate calibration of the pulse width, or it is just interesting to observe the system response against different pulse widths. For instance in CTA, the different cameras have different specifications. With the SRD design several circuit boards would be needed for that purpose. The generator here presented offers the possibility to modify the width pulse in an easy way, being even feasible to control it remotely.

On the other hand the SRD-based pulsers suffer from variations in time position of the output pulse due to temperature fluctuations. This is not present in the SOT (Signal on Transition) pulse generator, or at least in a much lesser extent.

Another limitation is encountered in the repetition pulse rate. The time required for charging and discharging the step recovery diode imposes a boundary in the maximum pulse repetition frequency.

Finally, this design is performed with standard components, and just one type of NPN transistor is used. That makes much easier its adaption to an integrated circuit manufacture process.

5.2 SOT pulser design

The design carried out is shown in the Figure 5.1. It is mainly composed by a current source, a resistor and four N-channel enhancement transistors. Two fixed voltages (V_1 and V_2) and one variable ($V_{control}$) are used to control the conduction and cut-off state of the transistors. The signal employed as $V_{control}$ is a low bandwidth pulse generator similar to the used in the SRD pulser.

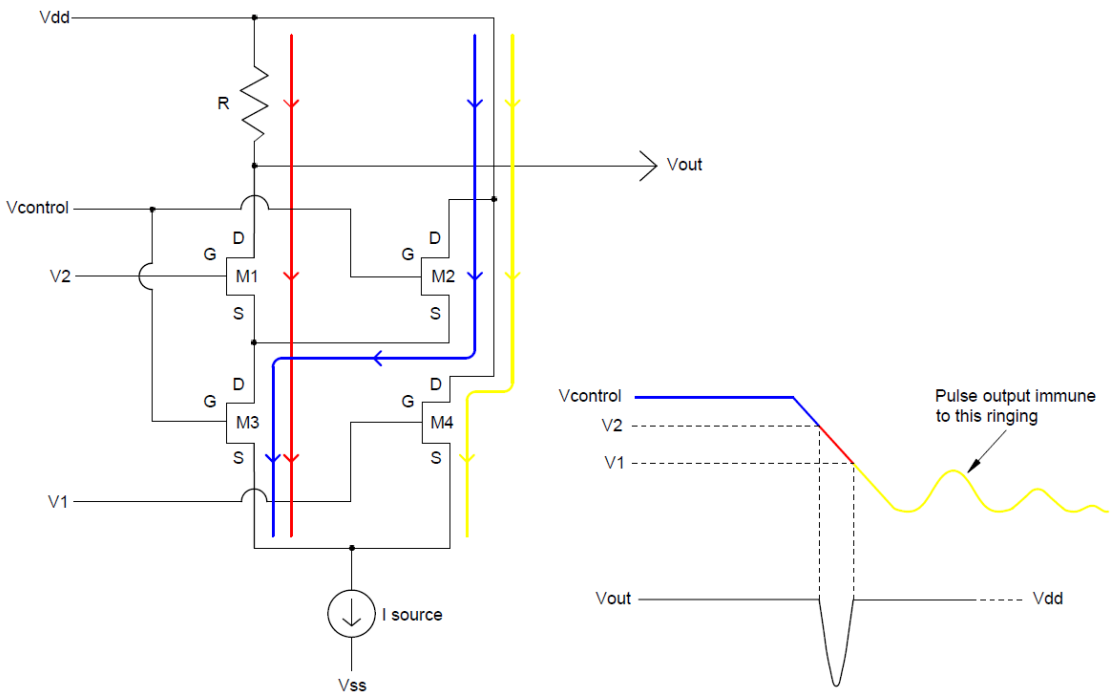

Figure 5.1 SOT pulser schematic

Initially $V_{control}$ is at a high level with a value greater than V_2, so transistors M2 and M3 are ON, while M1 and M4 are OFF (blue signal in Figure 5.1). When $V_{control}$ decreases to a value between V_2 and V_1, transistor M1 changes to conduction state and M2 to cut-off (red signal in Figure 5.1). Finally, $V_{control}$ goes under V_1 and consequently transistor M4 enters into conduction while M1 and M3 change to off state (yellow signal in Figure 5.1).

As deduced from the above operation, during the time the control voltage is between the fixed voltages V_1 and V_2, the current passes through the resistance R. Therefore a negative pulse is generated at the output of the circuit (i.e., at the drain terminal of transistor M1). This pulse is base-lined at the voltage V_{dd}.

Respectively, another pulse is created with the transition of the control signal from low to high voltages. The waveform used as control signal to drive the pulser is a square wave, so two output pulses are originated for each control pulse, one at the leading edge and other at the trailing edge.

These two output pulses can present different widths, depending on the control voltage rise and fall times, as it will be discussed later. If it is desired to have just one pulse (for example at the leading edge), it's enough with adding the circuitry necessary to allow the current source to work just when required and turn it off the rest of the time, so no current will flow through R.

One of the most important skills of this design is that the output pulse is immune to the ringing that the control signal can suffer at his high or low value, since the final pulse is formed just in the transition from both voltages. This is shown in Figure 5.1.

As it can be deduced from the design, the width of the pulses depends on the time the control voltage is between the voltages V_1 and V_2. Therefore it can be controlled by means of two different ways:

1) Moving closer or away the value of the voltages V_1 and V_2, so control voltage is less or more time between V_1 and V_2. As result, narrower or wider output pulses are obtained, respectively.
2) Changing the slew rate of the control signal, so in the same way lower slew rates will involve wider pulses, and vice versa.

The first possibility lets a minor margin of change, considering that if the voltages V_1 and V_2 are brought together or distanced too much, transistors may be biased into a non-desirable operation point. For this reason the second method will be realized. That's, voltages V_1 and V_2 will be fixed to a constant value and the output pulse width will be controlled by means of the control signal rise and fall times, which offers a greater range of feasibility.

Due to the fact that the design just contains resistors and the same type of transistors, an implementation into a single integrated circuit is much easier. However, for the analysis of the performance of the circuit, an implementation with discrete components has been carried out (Figure 5.2).

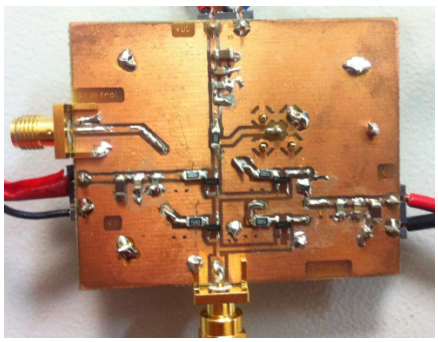

Figure 5.2 SOT pulse generator PCB

5.2.1 Current Source design

Current sources are commonly used in a wide variety of applications. In many of them it is desired to modify the value of the current in order to change the behavior of the circuit. In a laboratory framework, it is also very helpful to change the current value to perform tests. Unfortunately, a current source is not a common instrument available in all laboratories as for example voltage sources can be, and a reliable and fast to implement

design would be very helpful. Simplicity reduced space (few components) and low cost are also essentials features in any design.

For these reasons a variable current source based on a JFET transistor has been chosen [3]. This device has the characteristic to be on with no voltage difference between its gate and source terminals. Then, simply placing a variable resistor between the source and the gate will allow modifying the value of the current through the transistor. In particular, an N-channel JFET will be used. Also, there are a lot of different types of current sources designs, so another one can be implemented if desired [4][5][6].

In the Figure 5.3 the variable current source circuit is shown. When R1 and R2 are both 0 ohms, the gate and the source terminals of J1 are at the same voltage ($V_{GS} = 0\ V$) and JFET is on. As resistance increases, the voltage V_{GS} starts to drop and consequently the current decreases. If the value of the resistance (the sum of R1 and R2) continues increasing, the voltage difference between the gate and the source is more and more negative until the pinch-off voltage (V_P) is reached and the JFET is cutoff.

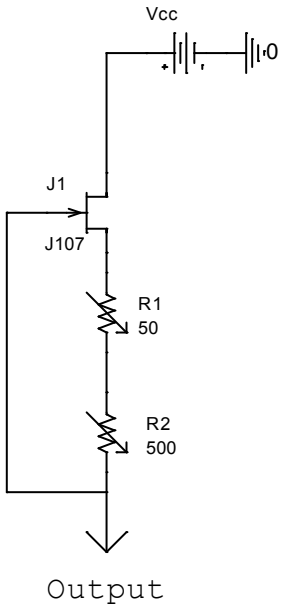

Figure 5.3 Variable current source circuit

R1 is used to limit the maximum current through the JFET. Due to the variations in the value of the drain-source saturation current (I_{DSS}) between transistors [5], a variable resistor has been chosen, so it is possible to calibrate the current source to the maximum current desired. Once R1 has been fixed, the value of the current source is changed from the minimum to the maximum by means of R2.

The value of R1 determines the maximum current. The value of R2 plus the value fixed for R1 determines the minimum current. In particular, the higher R2 is, the smaller the minimum current will be.

A current source with an operation range from a few milliamps to around 30-40 mA is required. That can be achieved setting R1 around $40\ \Omega$ and choosing a $500\ \Omega$ resistor for R2. According to the ORCAD simulation (Figure 5.4) it yields:

$R_{min} = R1 + R2 = 40\ \Omega + 0\ \Omega = 40\ \Omega \rightarrow I_{max} \cong 35\ mA$

$R_{max} = R1 + R2 = 40\ \Omega + 500\ \Omega = 540\ \Omega \rightarrow I_{min} \cong 2\ mA$

Current source range: [2, 35] mA

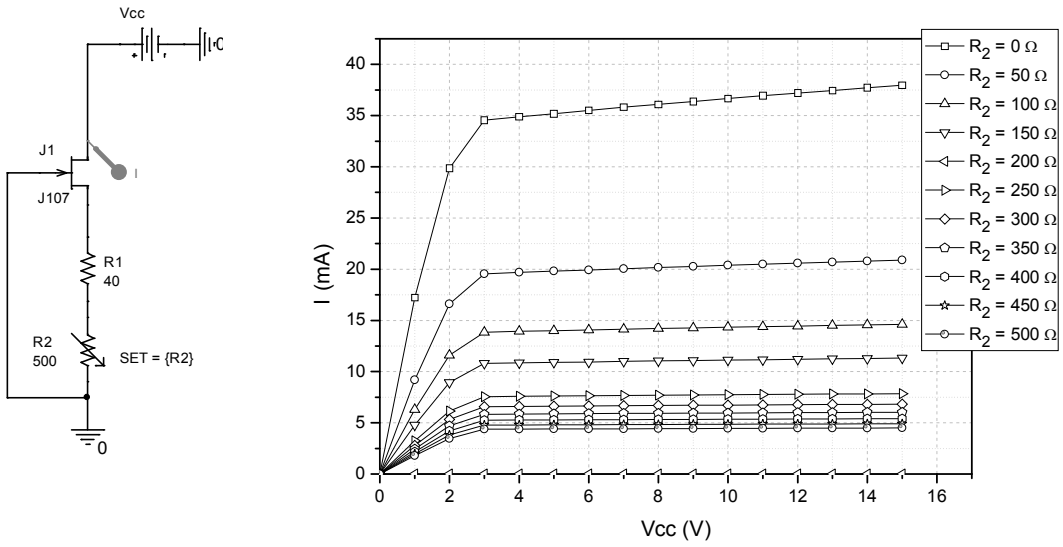

Figure 5.4 Left: Circuit schematic. Right: ORCAD Simulation result for R2 variable

As it can be deduced from I-V curve, the proper working of the current source occurs when JFET is in saturation operation mode. In this region, the current is kept fairly constant regardless the voltage required.

Another point that can be deduced from the simulation (Figure 5.4) is that there is not a linear relationship between the potentiometer position and the value of the current. One way to improve that linearity could be the use of a logarithmic potentiometer, employing the side which counteracts the non-linearity. Figure 5.5 shows the comparative between the use of a linear and a logarithmic potentiometer, results obtained by simulation. It can be observed that the response of the current source is almost linear in the most positions of the potentiometers (except at the end) when a logarithmic one is used.

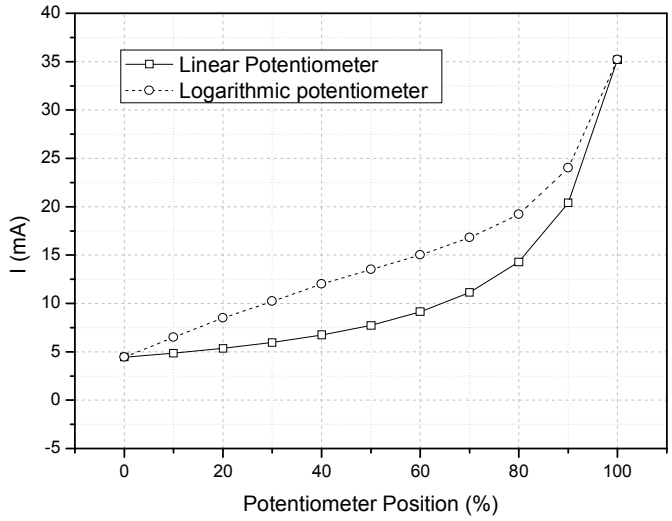

Figure 5.5 Logarithmic potentiometer vs linear potentiometer

5.2.2.1 Current source experimental outcomes

Two boards have been developed. A comparison between the simulation results and the experimental value of the two current sources is showed in the Table 6.1. In all the cases the value of the current is taken for a drain voltage (V_{CC}) of 10 V.

	$I_{DS}(mA)$		
R2 (Ω)	**Board 1**	**Board 2**	**Simulation**
0	54.5	40.1	37.3
100	18.1	13.6	14.5
200	10.0	7.9	9.1
300	7.4	5.7	6.8
400	5.5	4.2	5.4
470	4.6	3.7	4.8

Table 5.1 Current source values ($V_{CC} = 10\,V$)

The variations observed in the values of the current are mainly due to the fluctuations of I_{DSS} between transistors, as it was previously discussed. That demonstrates the need for the calibration variable resistor R1.

5.2.2 Negative voltage source

In the SOT pulser design negative voltages are required. To obtain that there are mainly three possibilities:

1. To use negative voltage regulators (LM7905, LM7912, LM337, etc…). Nevertheless, these components need a negative voltage input so this option is discarded.

2. To design a negative power supply by means of a transformer, diode bridge, regulators, etc…

3. To use charge pumps. These devices are DC-to-DC converters can provide negative voltages from positive ones. On the other hand they have the disadvantage that can just supply small currents.

As a compact design is desired and not a great amount of current is needed, a design based on charge pumps has been chosen. Among all the commercial charge pumps studied, the model TC962 from Microchip [7] has been chosen due to its high output current (80 mA) and its wide operation range (3 V to 18 V). Additionally, it has a power conversion efficiency of 97% and voltage conversion efficiency of 99.9%.

In the Figure 5.6 the circuit operation (left) and the implemented design (right) are shown. Internally, four transistors control the charge and discharge of the external capacitors. In the first part of the cycle the transistors SW1 and SW2 are turned on and the capacitor C_P is charged to the input voltage value. Next they are turned off and, after a short delay for preventing cross conduction, transistors SW3 and SW4 are switched on. Then, the charge in capacitor C_P is transferred to C_{INV} but with the polarity inverted.

This circuit is also very useful for testing procedures, as negative voltage power supplies are not common laboratory instruments. In this case, the SOT pulse generator design requires three polarizations references: $+V_{dd}$, Gnd, and $-V_{SS}$, (Figure 5.1) where V_{dd} and V_{SS} can be different and Gnd ones must be real ground because other equipment (as for example function generators) is going to be used for testing. Consequently, an independent negative voltage source is necessary.

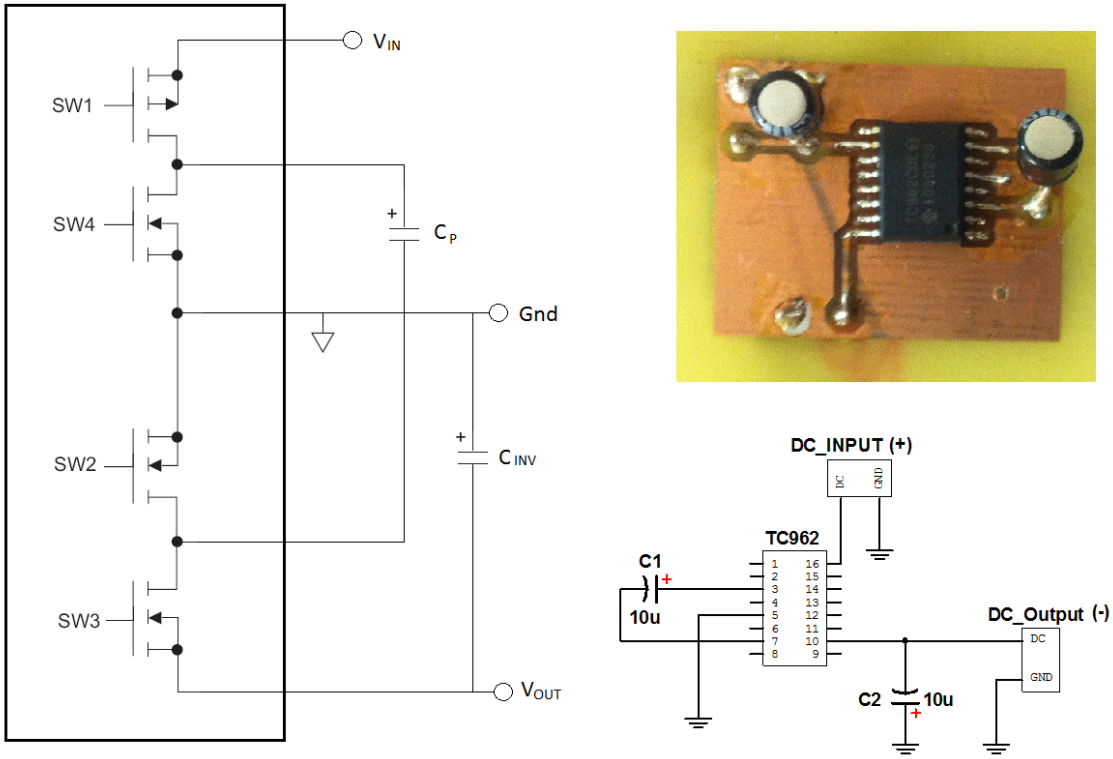

Figure 5.6 Charge pump: operation (left), design and implementation (right)

5.2.3 MOSFET biasing remarks

Some considerations have to be taken into account when working with MOSFET transistors. In Figure 5.7 the MOSFET model for switching applications is showed, which includes the most important parasitic components that affect to switching performance.

As it can be deduced from the Figure 5.7, parasitic input capacitances and inductances form a resonant circuit that can origin gate ringing, this is, high frequency oscillations on the gate to source voltage [8][9]. It is important to realize that the contribution to inductances value is for both inherent to MOSFET parasitic inductance and long printed circuit board traces (and sometimes this is the dominant). If necessary, gate ringing can be suppressed or at least damped by two ways:

- **Placing a resistor in series with the gate**, so Q factor is reduced. It has to be placed as close as possible to the MOSFET gate terminal. It is necessary to have in mind that there are already two more resistances taking part in the resonant tank: gate driver output impedance and the internal gate mesh resistance.

The selection of its value has an important trade-off: the higher its value is the better damping but also slower switching speed will be achieved. This is due to that the resistance

reduces the gate current, so charge / discharge times of the MOSFET input capacitance ($C_{iss} = C_{gd} + C_{gs}$) get longer, and consequently switching times are increased. Usually, a small value resistor is used.

In the case there are two or more MOSFETs paralleled, one resistance for each transistor is needed.

- **Making layout trace lengths the shortest possible** in order to minimize inductances and so Q factor. Also resonant frequency is increased. On the other hand, inductances values play a very important role in switching performance, as they slow down gate current and then the time to charge / discharge input capacitance (C_{iss}) gets longer. Shorter layout traces will be traduced in faster switching.

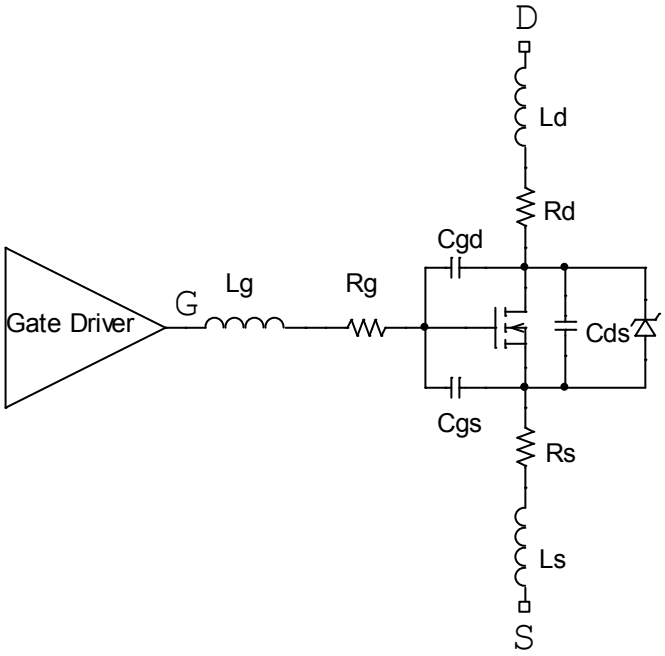

Figure 5.7 MOSFET model

5.3 SOT simulation and experimental outcomes

5.3.1 Simulation

The output of the pulse generator is the voltage drop produced across the resistor R when the current goes through it during the transitions of the control voltage signal (marker in Figure 5.8). An inverted pulse base-lined at the V_{dd} voltage is obtained.

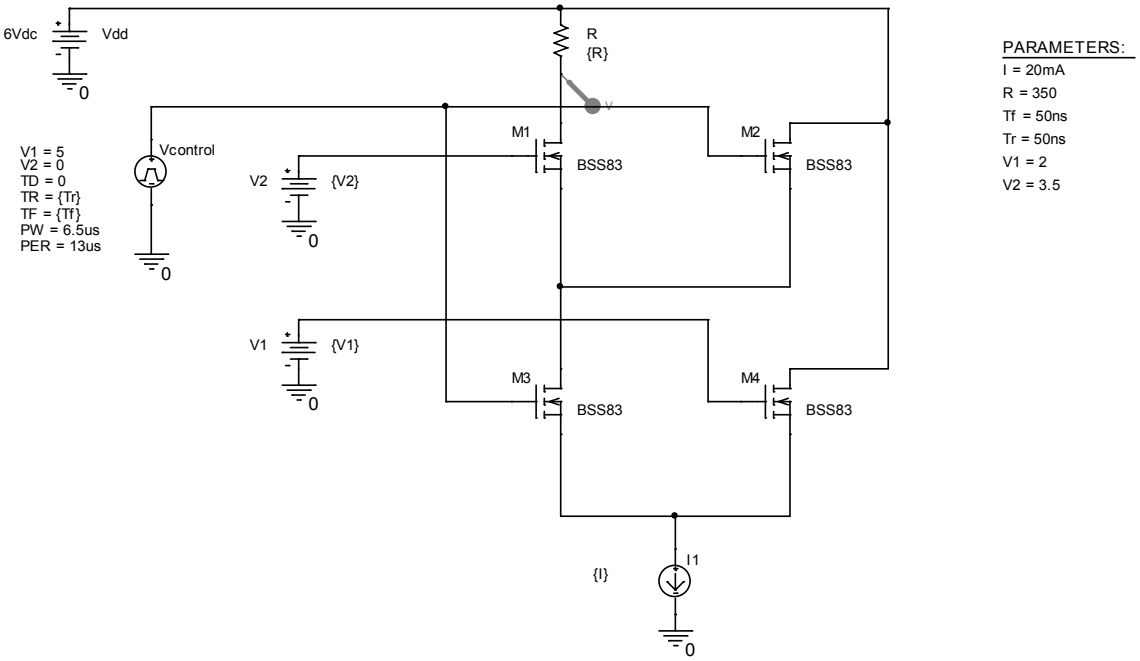

Figure 5.8 SOT pulse generator circuit simulation

The amplitude and width of the pulse can be modified by means of several parameters. Figure 5.9 shows the dependence of the pulse shape with the most relevant variables of the design. The simulation has been carried out performing a sweep of the variable in study and keeping fixed the rest.

From the bottom graphic of Figure 5.9 it is deduced that the longer the rise time is (T_r), the wider the pulses are. This is because the control signal stays between the voltages V1 and V2 during more time, as the slope is minor. Consequently the time there is current flow across the resistor R is greater. The amplitude remains constant for all the values of the rise time. These conclusions are equally valid for the falling time. In the same way the greater the voltage difference between V1 and V2 is, the wider the pulses are. In this case the amplitude is also increased.

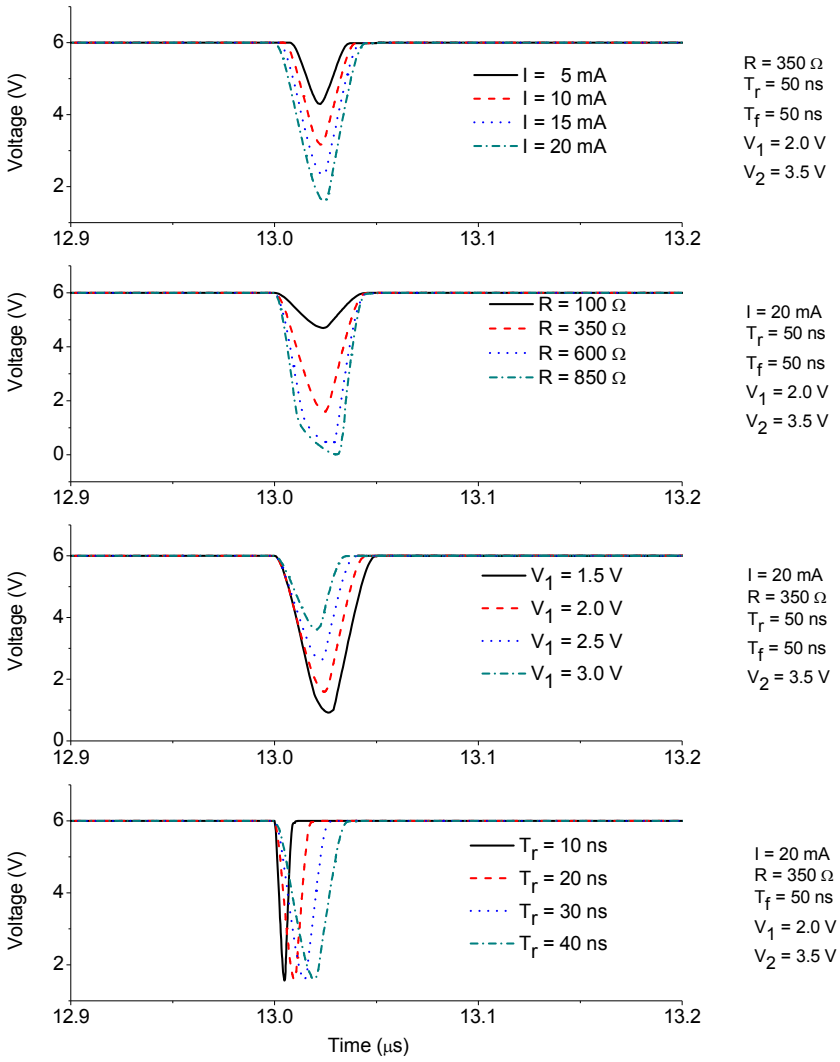

Figure 5.9 SOT pulse simulation obtained varying, from top to bottom: the current source value (I), resistance (R), M1 gate voltage V_1 and the rise time (T_r)

Higher values of the output resistance R yield in higher amplitude pulses. It can be noticed that there is a point from which the shape of the output pulse starts to be distorted and there is a loss of symmetry. This situation takes places when there is an excessive voltage drop across the resistor and the transistors are away from its operation point. For this reason the value of this resistor will be fixed to 330 ohms. Finally, the value of the current source has also a direct effect in the output pulse (top of Figure 5.9). Higher values of the current source will result in higher amplitude pulses but also wider pulses.

As it can be observed, there are several parameters that have influence on the amplitude and the width of the output pulse. The aim is to design a pulse generator with constant amplitude and variable width.

Among all the possibilities, it can be inferred from above simulations that the best way to change the width of the pulse, keeping the amplitude constant and without interfering in the circuit behavior is by means of varying the slew rate of the control pulse.

The rest of the parameters will be fixed to a constant value. Even though it is possible to control the width of the output pulse by varying for example the voltage difference between V1 and V2, or even modifying the value of the current source, two important aspects have to be taken into account:

- Varying these parameters the pulse amplitude will also change, which is not at all desirable. The amplitude of the pulse generator must be kept constant against width changes.

- The margin of change of these parameters is not very large. If we deviate too much from the working point, we can enter into a non-desired operation point, where the MOSFETs are not biasing as required, causing the pulse generator to fail.

As previously discussed, controlling the width pulse by means of the slew rate will prevent from the above problems, as it maintains the amplitude constants and does not interfere in the biasing point of the transistors.

That's why these parameters will be adjusted initially to a fixed value and kept constant.

5.3.2 Experimental results

In order to make measurements of the pulse generator output, a DC-block has to be placed for avoiding the flow of direct current towards the oscilloscope, what would cause an improper behavior. A broadband performance and a matching to the 50 ohms input impedance of the oscilloscope are critical parameters for visualizing the output pulse free of distortion. The model selected has been the coaxial DC-block BLK-89+ from Mini-Circuits [10], which features a wide band from 0.1 MHz to 8 GHz and a low insertion loss.

The values of the SOT pulse generator has been fixed to the following: $R = 330\ \Omega, V_{dd} = 6\ V$, $V_1 = 2\ V$ and $V_2 = 4\ V$. The current source board has been adjusted to 32.5 mA being supplied by the negative voltage source board which is fixed to an output value of -4.5 V. A 0 to 7.5 V amplitude and 400 ns periodic pulse is used as control voltage, which has been produced by means of the function generator model Tektronix AFG3252. The high level of the control voltage has been chosen several volts greater than V_2 in order to guarantee the correct turn off of the transistor M1 when the voltage control level is at high state. The measurements have been taken for various values of the leading and falling edge times (Figure 5.10).

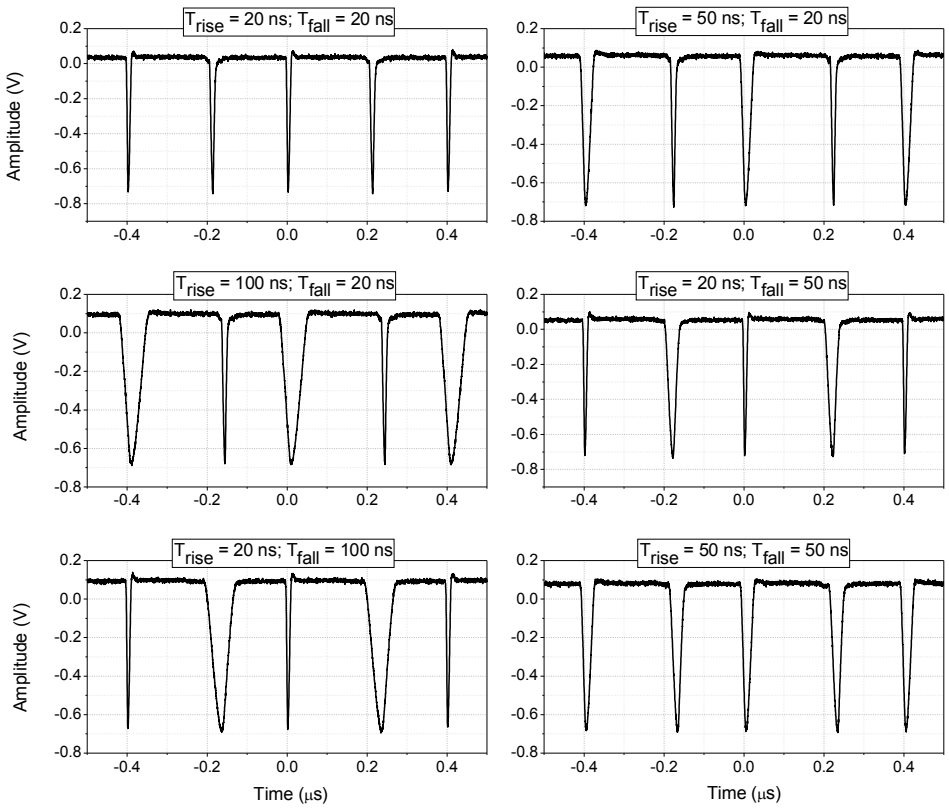

Figure 5.10 SOT pulse generator output

The dependence of the pulse width with the transition times is observed in the Figure 5.10. Thus, for values of 20, 50 and 100 ns are obtained FWHM of 7.1, 19.4 and 38.5 ns, respectively. These pulses occur in both the rise and fall transitions. Then, it is possible to achieve alternated pulses with different widths. As previously remarked, the SOT generator output are inverted pulses base-lined at the voltage V_{dd}.

If an unique pulse is required, it is enough with switching on and off the current source when necessary. That is, if the pulse occurred in the rise transition is desired, the current source has to be turned off during the fall edge. In the same way, it is possible to control the time the pulses appear by just controlling the operation of the current source.

From Figure 5.10 can be remarked that the amplitude of the pulses is much minor that the expected from the simulations (Figure 5.9). This is due to the 50 ohms input impedance of the oscilloscope, as the SOT output pulse requires a high impedance load.

With this circuit pulses from up to 1.4 ns for transition times of 5 ns have been achieved, but the wave shape starts to loose amplitude and to be distorted. Below 5 ns the pulse has lost almost all its amplitude and shape. To obtain much narrower pulses free of distortion it is necessary to implement this design in an ASIC to eliminate parasitic

capacitances and inductances coming from the PCB traces and from discrete devices package.

Finally the jitter of the pulse width is measured (Figure 5.11). It has been taken the pulse corresponding to the rise edge for a transition time of 20 ns. The pulse related to the trailing edge has been erased adjusting a fall time of less than 5 ns. A jitter of 168 ps for a pulse width of 7.12 ns has been obtained. No measurements of the repetition frequency jitter have been carried out as the result will just give information about the function generator used as control signal, and not about the pulser circuit here presented.

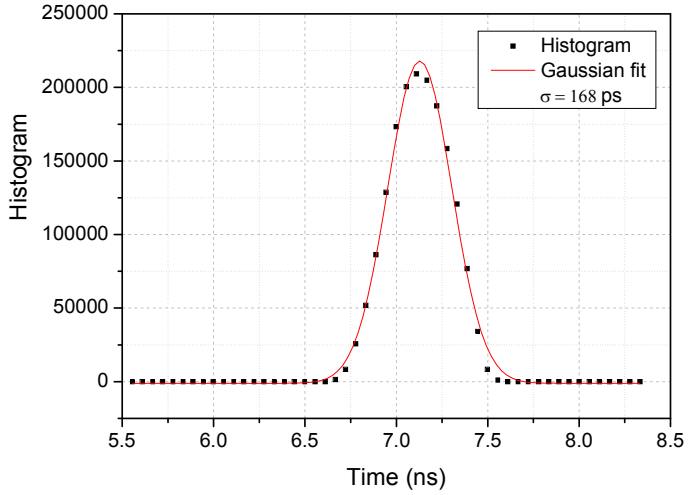

Figure 5.11 SOT pulse width jitter

5.4 Matching stage

The purpose of this circuit is multiple and it has to comply with demanding features:

- It has to invert the output pulse and also to filter the DC signal. That is, the final pulse must be referenced to zero voltage level and to have a positive amplitude.

- Its input impedance has to be high for preventing the flow of current through it.

- Its output impedance has to be low in order to be matched to a 50 ohms load.

- The output current has to be high to connect it to a low impedance load providing a high amplitude pulse output.

- And finally and essential, this stage has to feature a high bandwidth for transmitting the entire pulse.

All these features are fundamental in order to achieve high amplitude pulses free of distortion. A high speed instrumentation amplifier has been chosen for that purpose (Figure 5.12) [11][12]. This circuit is composed by three operational amplifiers and several resistors. Also bypass capacitors from supplies to ground are essential to achieve a good performance.

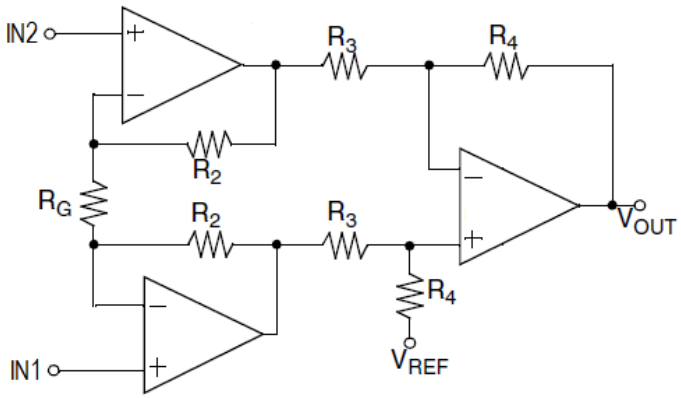

Figure 5.12 Instrumentation amplifier

The output of the instrumentation amplifier is determined by the following equation:

$$V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{2R_2}{R_G}\right)\left(\frac{R_4}{R_3}\right) + V_{REF}\left(\frac{R_4}{R_3}\right) \quad (5.1)$$

In this design no signal amplification is needed. To get an overall unity gain resistors R_2 are short-circuited (i.e. 0 ohms resistors), R_G is not placed and the values of R_3 and R_4 are made equal. Additionally the reference voltage is connected to ground.

The input signals are connected to the non-inverting input of the amplifiers, which act as buffers. This first stage provides then high impedance and load isolation, critical factors for the SOT pulser output.

Next there is a difference amplifier which subtracts both signals. Here the inversion of the pulse and the filtering of the DC signal are achieved (remember the SOT pulse is base-lined at the voltage V_{dd}). This is accomplished by connecting the DC voltage V_{dd} to the input IN1 and the output of the SOT pulse generator to IN2.

The operational amplifiers to use must be carefully selected because of the requirements of the application. There is an important trade-off between bandwidth and power handling. Usually the faster devices have a narrower operation voltage range. In the design here presented both characteristics are necessary. First, the high bandwidth is needed to be able to transmit very narrow pulses. Second, the SOT output pulse presents a considerable DC voltage level.

For the first stage of the instrumentation amplifier high input impedance is required. The op amps with higher impedance values are the FET input amplifiers, which present impedances in the $G\Omega$ range. Nevertheless they are not extremely fast. On the other hand, the faster operational amplifiers in the market are the current feedback ones. Unfortunately its input impedance is very small.

The definitive model of amplifier chosen for the first stage has been the ADA4857 from Analog Devices [13]. This is an ultralow distortion, low noise and high speed op amp that features an input impedance of several $M\Omega$, a bandwidth of 750 MHz and a slew rate of 2800 $V/\mu s$.

Next, for the remaining op amp (the difference amplifier), the same model cannot be used as it can just provide 50 mA of output current. Then, for a 50 ohm load a pulse of just 2.5 V of amplitude would be obtained. As a high input impedance is not required here, a current feedback amplifier has been chosen. In particular, the low distortion and very high speed amplifier AD8009 from Analog Devices [14] has been selected. It has a bandwidth of 1 GHz, a slew rate of 5500 $V/\mu s$ and an output current of 175 mA. In summary, the two ADA4857 provide high input impedance and the AD8009 provides high output current, featuring both high speeds. Figure 5.13 shows the definitive design of the instrument amplifier and its connection with the SOT pulse generator. Next, Figure 5.14 shows the matching stage once fabricated. A summary of the components used for the SOT pulse generator and the matching stage can be found in Appendix D.

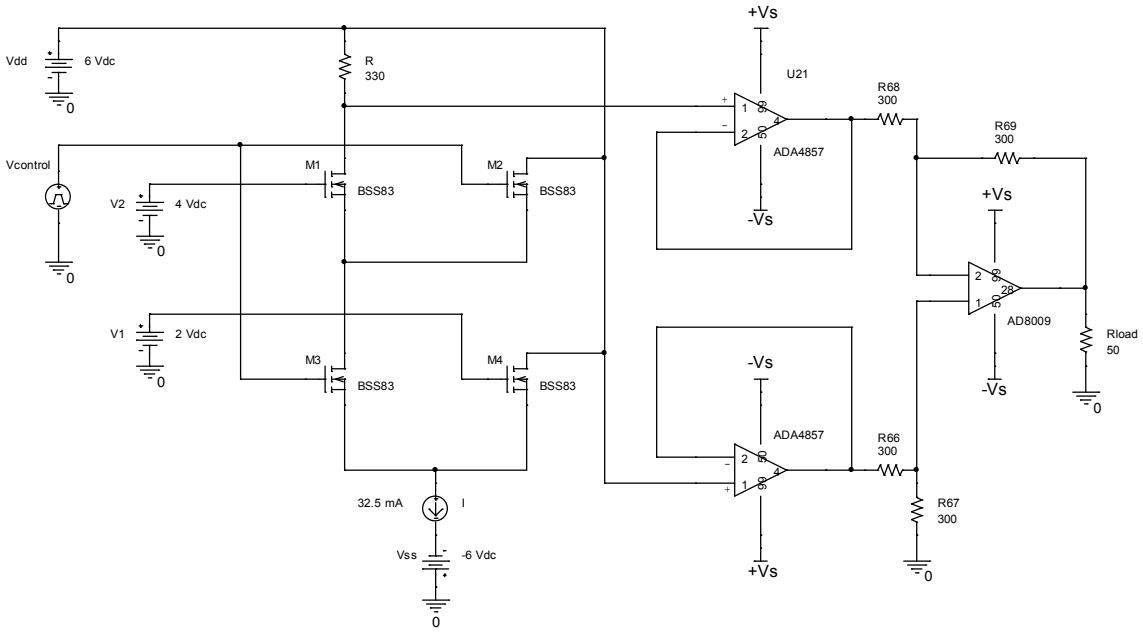

Figure 5.13 SOT pulse generator plus matching stage schematic. All supply capacitors are omitted.

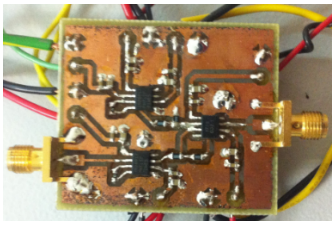

Figure 5.14 Matching stage PCB

Figure 5.15 shows the SOT generator output pulse corresponding to the schematic of Figure 5.13, that is, placing the matching board between the pulse generator and the oscilloscope. In order to compare with the previous measurements the same control signal as that one used for obtaining the results of Figure 5.10 has been employed here.

The three op amps have been biased with similar voltage values. The positive supply rail $+V_S$ is adjusted to 7 V, and the negative rail $-V_S$ to -2.5 V. They have been selected several volts over and below the maximum and minimum voltages of the required final pulse, respectively, in order to adequate the pulse within the input and output voltage ranges of the op amps [15].

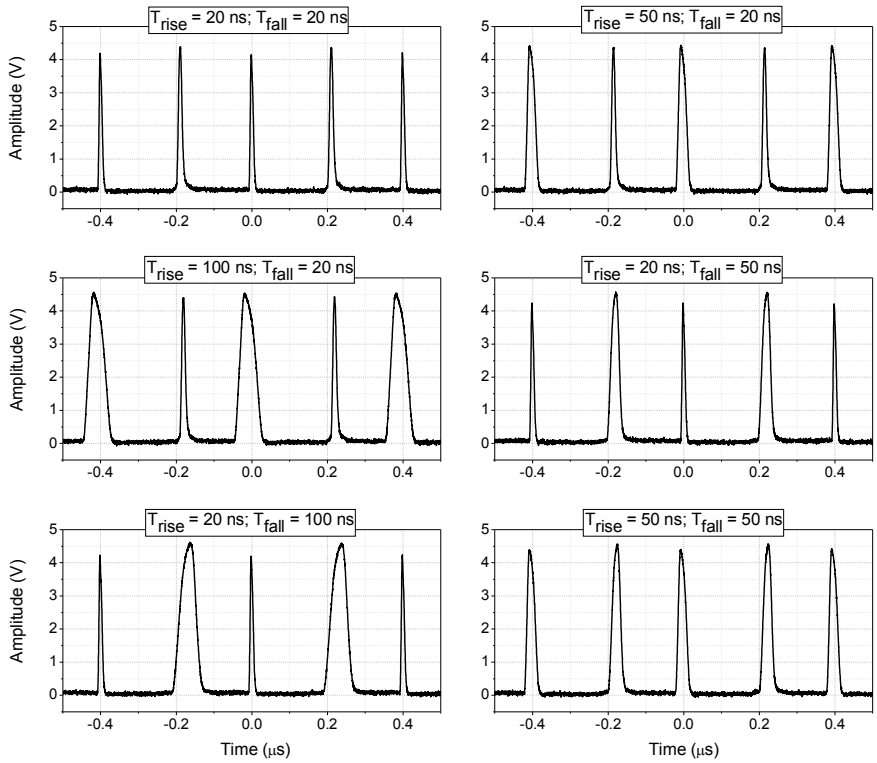

Figure 5.15 SOT output pulse with the matching stage. Measurements carried out for several values of the transition times.

Pulses base-lined at zero volts with amplitudes of more than 4 V have been achieved. Likewise, pulse widths of 8.5, 22.9 and 45.0 ns have been obtained for transition times of 20, 50 and 100 ns, respectively and for both the rise and fall edges. As it can be remarked, the matching board does not almost widen the pulses, as it has to take into account that the amplitude is more than six times greater. It is very important to emphasize that the matching stage does not amplify the signal as it has unity gain, it just adapt the SOT pulser output. If greater amplitude pulses are desired, the matching stage could be also used as amplifier.

Finally, a jitter of 149 ps and a pulse width of 8.47 ns have been measured for the pulse corresponding to a transition time of 20 ns in the rise edge, what is shown in Figure 5.16. As above, the other pulse has been avoided adjusting a falling edge of less than 4 ns. This jitter is very similar to the obtained without the matching stage.

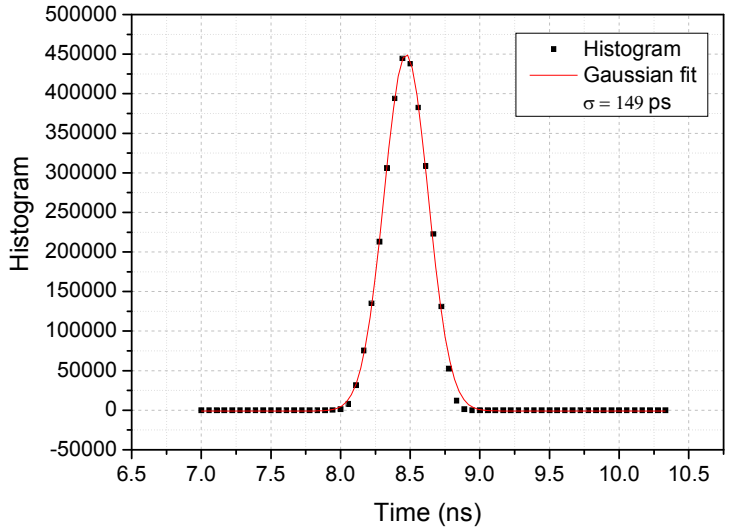

Figure 5.16 SOT pulser plus matching stage pulse width jitter

Other designs could have been implemented. A reduced version of the instrumentation amplifier is shown in Figure 5.17. With this configuration the high impedance and load isolation required for the output pulse is achieved by means of the first ADA4857 op amp. The other input of the instrumentation amplifier, V_{dd}, is connected to the high impedance non-inverting op amp input with what load isolation is guaranteed. Very high impedance is here not necessary so the AD8009 can be used.

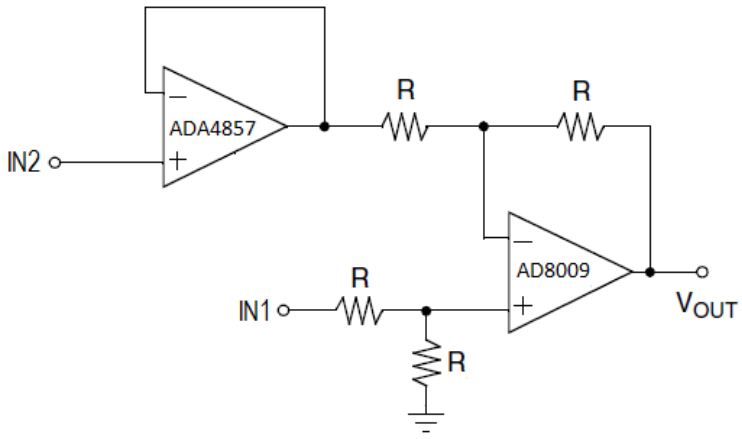

Figure 5.17 Matching stage reduced version

Another possibility would have been an impedance matching pad from for example 1 MΩ to 50 Ω. In the market it is very common to find matching pads from high impedance to 75 Ω, but not to 50 Ω, so it would be needed to be designed.

5.5 Transition Time Control Circuit (TTCC)

The aim of this section is to design a variable rise and fall time pulse generator. The output of this circuit will be connected to the control voltage input of the SOT pulser. As it was previously shown, longer falling or rising times will result in wider pulses, and vice versa.

The basic principle of the circuit is based on the charge and discharge of a capacitor (Figure 5.18) by means of two current sources: one for charging (I_C) and another for discharging (I_D) [16][17]. Consequently, rise and fall times are independently controlled. The constant current guarantees a linear rate of change of the voltage across the capacitor ($dV/dt = I/C$).

Transition times are therefore dependent on the values of the capacitor and the current. The capacitor will be fixed to a constant value but the current will be variable, so modifying the value of the current source will change the slope of the output pulse.

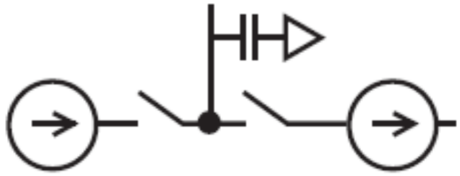

Figure 5.18 Variable transition time schematic

Nevertheless, it is needed to carry out some modifications to the design of Figure 5.18. The main issue presented in that circuit is the long times required for turning on and off the current sources at each cycle. That can cause two non-desirable effects:

- A large time limitation. It would hamper from achieving very abrupt slopes (low transition times).

- Non-linear slopes. A long time for reaching the fixed value of the current involves a distorted waveform. During that time the current is not constant and consequently neither the rate of charge/discharge of the capacitor is. Then in that interval of time the slope of the voltage across the capacitor (i.e., the output pulse) is different from desired.

The level of distortion depends on both, the time the current is not constant and the value of the output capacitor. The more time the current source is out of the fixed value, the larger is the percentage of the output ramp that is not linear. On the other hand, a greater capacitor means more time to be charged / discharged, and consequently a minor percentage of the rise or fall ramp affected (as the total time is increased). On the contrary, it also means longer transition times.

As deduced from Figure 5.18, the current in the capacitor must be continuously switched on and off in order to allow the change between charge and discharge current sources. Then there is a transition time that is unavoidable and inherent to the design. Nevertheless as previously discussed, the longer times are the ones needed to turn on and off the current sources. Therefore, if it is achieved to keep both current sources always active, and depend just on the switching of the transistors, rise and fall times can be greatly reduced.

A four transistor design (Figure 5.19) is carried out in order to keep both current sources always on. During the rising edge the transistors M2 and M3 are on (red line). The transistor M2 allows the pass of the current coming from the top current source to charge the output capacitor. Transistor M3 creates a path to ground for the discharge current source in order to keep it active. Respectively, during the falling edge transistors M1 and M4 are on (blue line).

Also, two diodes have to be added in order to limit the low and high voltages. Otherwise the voltage would increase (or decrease) until very high values and some components would be damaged. In order to obtain pulses from 0 to 7.5 Volts, a diode Schottky and a 7.5 V Zener diode are used. Other amplitudes can be obtained by simply modifying the value of the Zener, depending on the amplitude required. Other types of designs can be developed, such as those reported in references [18], [19] and [20].

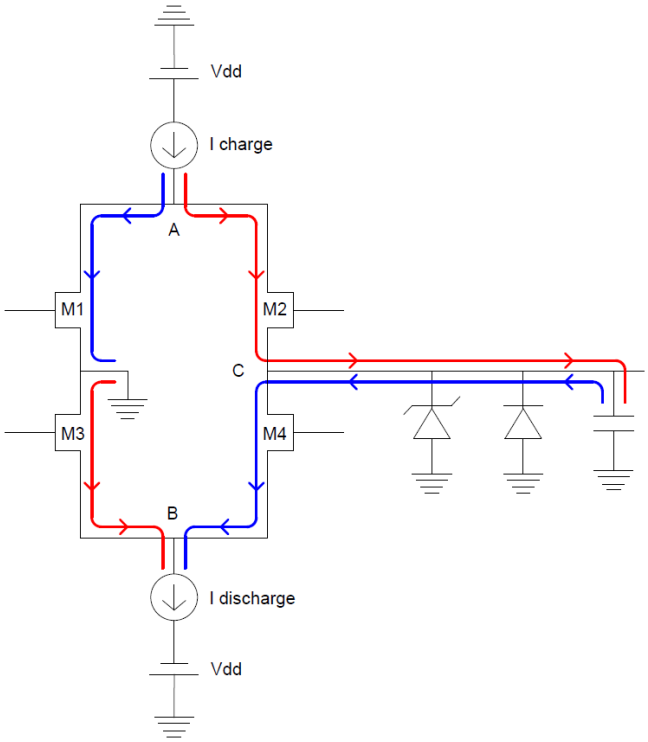

Figure 5.19 Variable transition time circuit final design

5.6 TTCC control

The control of the transistor switching behavior does not result an easy task. Apparently the design looks like a simple H bridge, but actually it is completely different. The path of the current is not the same and the voltages are not kept constant at the reference points. In the variable transition times pulse generator, the changing voltage at the output and the use of constant current sources cause that the voltages at points A, B and C are not constant. Consequently those points cannot be taken as reference for the transistors control.

The aim is to control all the transistors state by means of just one 0 to 5 volts low bandwidth pulser (same as used in the SRD pulser design). There are mainly two alternatives to achieve that:

1. The use of operational amplifiers to adapt the value of the low bandwidth pulser to the input voltage needed for controlling each transistor.

2. The use of different type of transistors whose operation range is compatible with the input and output voltages required for each switching cycle.

One of the greater difficulties in the TTCC control is located on the right side of the design (this is M2 and M4), where the voltages are not constant so the transistors cannot be referenced to a fixed point.

The first option solves that complication using the op-amp in a non-inverting adder configuration. Adding the output voltage to the control signal makes possible to reference the transistors to the output, since the gate signal is adapted to the output variations. On the other hand, thanks to the versatility offered by the op-amps, a greater variety of transistors can be employed.

Nevertheless it presents some disadvantages:

- Connecting the output voltage to the op-amp input can degrade the quality of the output signal. Even if the input impedance of the op-amp is very high, there is a little consumption of current. That can cause undesirable effects in the charge of the output capacitor, especially when working with the small capacitances necessary to achieve high slopes.

- Depending on the operation performed and the output voltage range, the time of the four op-amps can differ significantly.

- A higher cost due to the op-amps and more complex circuits

For all the above reasons and in particular due to the loss of isolation between the output and the rest of the circuit, the second option has been chosen. The selection of the transistors has to be adapted to the input and output voltages required. The ideal choice of transistors is the next:

Transistor M1: NMOS (BSS83)

Transistor M2: PMOS (BSS84)

Transistor M3: PMOS depletion

Transistor M4: NMOS (BSS83)

Unfortunately it has not been possible to find a P-channel depletion MOSFET in the market. For that reason it has been substituted by a JFET whose behavior is also compatible with this application. In particular the JFET J175 is used. In the Figure 5.20 the circuit schematic is shown.

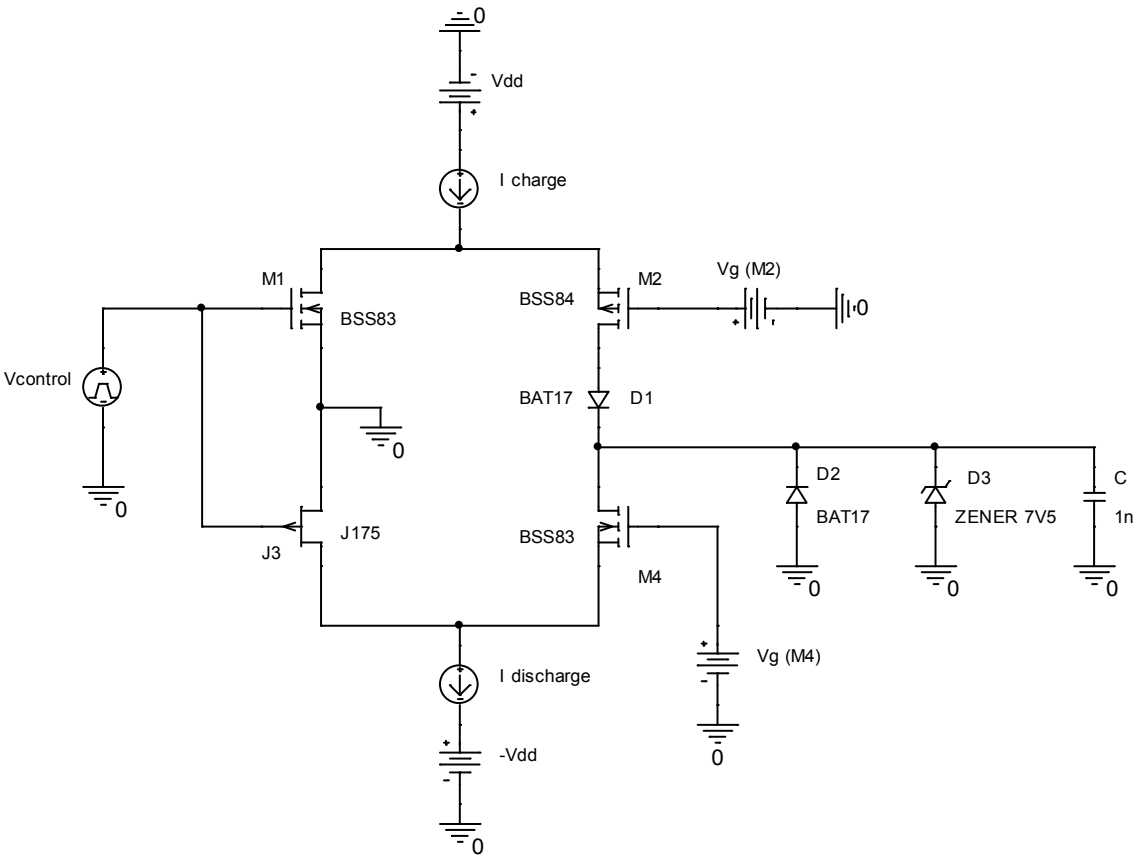

Figure 5.20 Schematic of the variable rise and fall time pulse generator

On the left side of the circuit transistors M1 and J3 have their source terminal connected to ground. Then, both of them are straightaway controlled by the signal received on their gates. A low bandwidth pulser is used as signal control. When it is high (5 V), NMOS M1 is on as $V_{GS} > V_T$. On the other hand JFET J3 is off due to $V_{GS} = -5\,V$. This is the great advantage of using different technologies transistor, with just one same signal it is possible to control several transistors in the desired way.

Regarding to the right side of the circuit, transistors switching is not so intuitive. M2 and M4 are fixed at a constant value, and they are switched from one state to other as explained in the following sub-section.

5.6.1 M4 transistor

In order to determine the gate voltage to be applied to M4, it is needed to know the voltage drop presents in J3 (V_{DS}(J3)), when it is gone through by the maximum current intended to be used.

That's, according to the I-V curve obtained from ORCAD simulation (Figure 5.21), the voltage drop across J3 when it is ON ($V_{GS} = 0\ V$) is about 3.2 Volts for a value of the current source of 30 mA. A value of -4 V is then chosen for biasing the gate terminal of M4 transistor. The use of higher currents is not at all recommended because of in the saturation region small changes on the current involve large voltage drops on J3, as can be deduced from Figure 5.21.

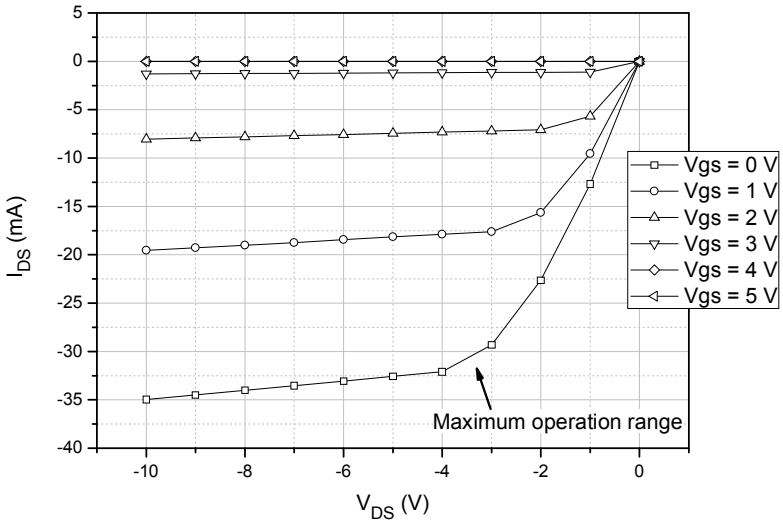

Figure 5.21 JFET J175 I-V characteristic curve

Then, J3 and M4 switching is explained next:

+ When the control signal is at low level (0 V), J3 is on. The maximum voltage difference between drain and source terminal is reached when the value of the current is the higher allowed. An upper limit of 30 mA was chosen, which correspond to about $V_{DS}(J3) \cong -3.2\ V$. The drain of J3 and the source of M4 are both connected together so it yields,

$$V_{GS}(M4) = V_G(M4) - V_S(M4) \leq -4\ V - (-3.2\ V) = -0.8\ V$$

Then, M4 remains off for the entire current source range.

+ When the input pulse change to high level (5 V), transistor J3 is immediately taken into cutoff. The voltage in the terminal source of transistor M4 (i.e. the top of the discharge current source) starts to increase negatively trying to keep the current level constant. In the current source used in this project which is based on a JFET and a resistor, the rise of the voltage $V_S(J3)$ is caused by a drop of the voltage between the drain and source of the current source JFET. When the thevenin voltage is reached transistor M4 is turned on:

$$V_{GS}(M4) = V_G(M4) - V_S(M4) = -4\ V - (-|V_S(M4)|) = -4\ V + |V_S(M4)|$$

$where\ |V_S(M4)|\ increases.$

As can be deduced from the above analysis, the fixed value applied to the gate of transistor M4 depends on both the I-V curve of the transistor used and the maximum value of the current source. Also slight differences can be found among transistors of the same model. In conclusion, all these reasons must be taken into account to adjust the gate biasing of transistor M4.

5.6.2 M2 transistor

It is proceeded in a similar way as with transistor M4. The current source corresponding to the discharge path of the output capacitor (i.e. the one that controls the fall time) was limited to 30 mA because of the characteristics of the transistor J3 used (J175). In order to homogenize the variation range of the current sources, and consequently the minimum and maximum pulse width, the charge current source is also limited to around 30 mA. However, according to the IV characteristic curve of transistor BSS83 (easily by simulation), if it is required it would be possible to use higher values of the current without involving an excessive increase of the voltage drop across transistor M1.

From the simulation of the BSS83 it is obtained that the drain to source voltage $V_{DS}(M1)$ for a current lower than 30 mA and a gate voltage $V_{GS}(M1)$ of 5 V is less than 1 V. Therefore the gate voltage of transistor M2 is fixed to 1 V.

The operation of the upper part of the design is explained next:

+ When the control signal pulse is high (5 V) transistor M1 is on. The maximum voltage at the drain of M1 (i.e. the source of M2) is less than 1 V, reached with the highest value of the current source. Consequently transistor M2 is off.

$$V_{GS}(M2) = V_G(M2) - V_S(M2) \leq 1\,V - 1\,V = 0\,V$$

+ When the control pulse change to low level (0 V) the transistor M1 is cutoff. Because of that the voltage at the source terminal of M2 starts to increase since the current source tries to maintain the value of the current. Once the gate to source voltage in transistor M2 reaches its thevenin voltage, it changes to on state.

$$V_{GS}(M2) = V_G(M2) - V_S(M2) = 1\,V\ - V_S(M2)\ \leq V_T = -|V_T|$$

where $V_S(M2)$ gets higher until the operating point is established.

Unlike the operation of the low part of the circuit (i.e. J3 and M4 switching), there is an added problem. It is started from the situation in which the output capacitor is completely charged (about 5 V) and transistor M1 is cutoff and M2 is on. When the switching of the input control pulse occurs, M1 changes to on and M2 changes to cutoff. During that transition there is a moment in which the voltage at the output capacitor (the drain of M2) is greater than the voltage at the source of M2 (A point in Figure 5.19). That makes the transistor M2 to be inversely biased and consequently there is a brief interval of time where

the current is driven in a non-desired direction (from output capacitor towards the upper part of the circuit).

This problem is simply solved placing a diode between the drain of transistor M2 and the output capacitor.

5.7 TTCC experimental outcomes

Figure 5.22 shows the final schematic of the implemented circuit. The control voltage (left most side of the circuit) used has been the same type of low bandwidth pulse generator as the employed in the SRD pulser design, which is based on a Smith trigger inverter.

The load connected to the output of the TTCC circuit must imperatively feature high impedance. Otherwise the output capacitor of the TTCC circuit will be discharged through the load path resulting in an improper working. The circuit implemented is shown in Figure 5.23. The current sources, based on a JFET, have been built in independent boards.

For taking measurements of this circuit two oscilloscopes are available in the laboratory: a Tektronix TDS3052 (500 Mhz, 5 GS/s) and an Agilent Infiniium DSO81204B (12 GHz, 40 GSa/s). Although the first one features a minor wide-band, it has the possibility of selecting the input impedance between 50 Ω and 1 $M\Omega$. For this reason this one has been selected to perform the measurements. The model DSO81204B would be just possible to be used here in combination with a high impedance probe, in order to minimize the interaction with the TTCC circuit. The high speed probe model Agilent 1131A would be an option. Unfortunately, it is not available at the laboratory.

Regarding the value of the output capacitor, it has to be large enough to not be affected by the input capacitance C_{iss} of the SOT generator MOSFET transistors. A value of 1 nF has been chosen so it is almost not influenced by the 3 pF input capacitance of the two BSS83 (1.5 pF for each transistor). Nevertheless, there is a significant trade off since the minor the value of the output capacitor is, the faster the transition times achieved are. A summary of the components used for the Transition Time Control Circuit can be found in Appendix D.

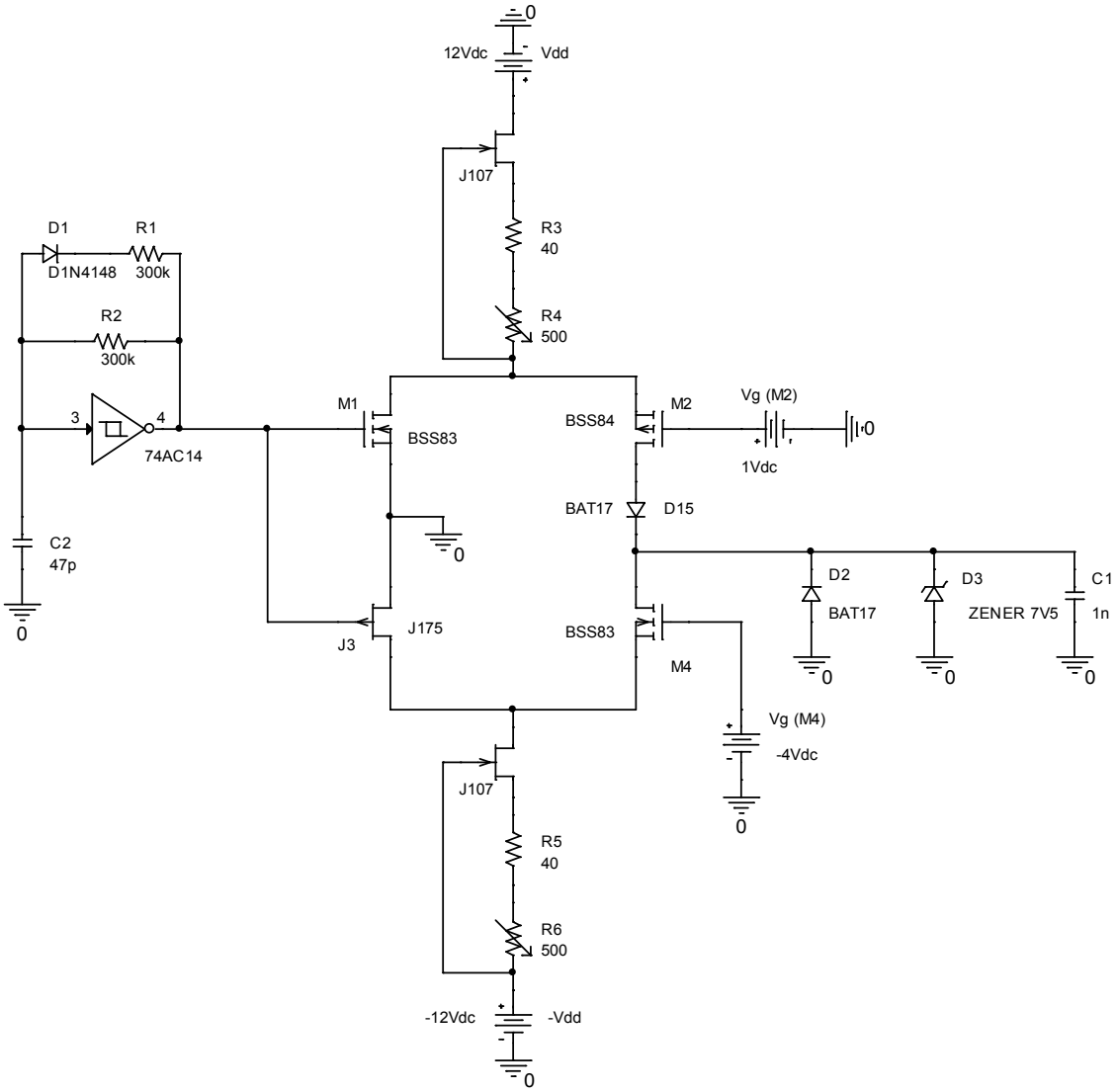

Figure 5.22 TTCC circuit schematic

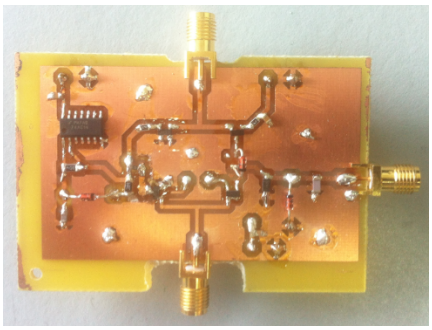

Figure 5.23 TTCC board

Figures 5.24 and 5.25 show the working of the TTCC circuit for various values of the current sources. The measurements have been obtained by means of the Tektronix TDS3052 oscilloscope in a 1 $M\Omega$ configuration.

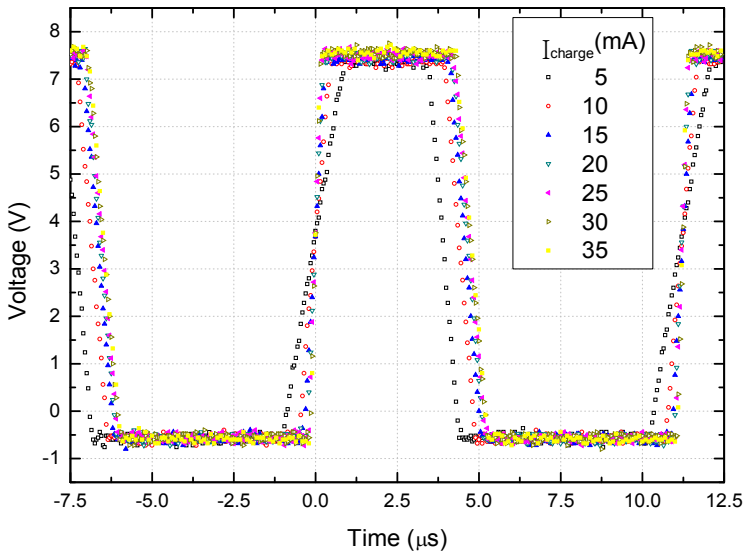

Figure 5.24 Leading edge transition time. $I_{discharge}$ fixed to 10 mA. I_{charge} variable from 5 to 35 mA.

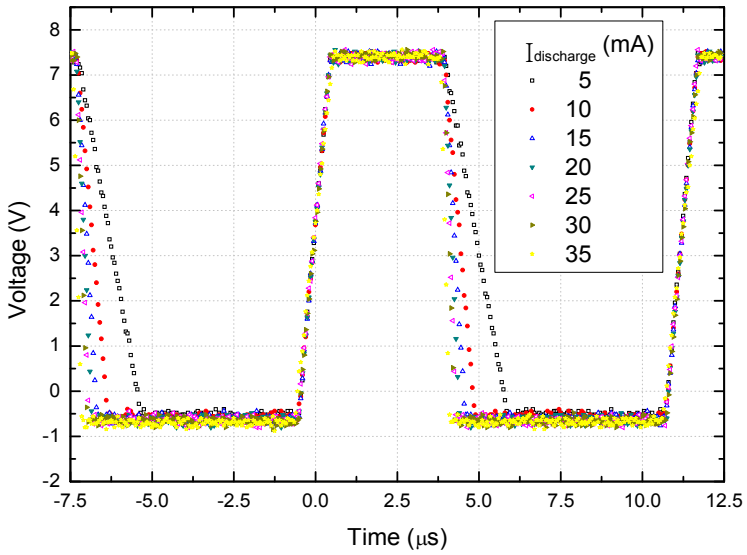

Figure 5.25 Falling edge transition time. I_{charge} fixed to 10 mA. $I_{discharge}$ variable from 5 to 35 mA.

Transition times from 250 ns to 1.8 µs have been achieved for both rise and fall edges. As above discussed, faster transition times can be obtained by decreasing the value of the output capacitor. Nevertheless, in this work some oscillations have started to be noticed with values under the nF. Consequently, a deeper analysis should be carried out in order to determine the cause of such oscillations and be able to reduce the value of the output capacitor. However, that is away of the scope of this thesis since the main intention was to provide a compact and easily adjustable design of variable transition time circuit. Possible improvements of this circuit are left open for future works.

Finally it is important to remark that when using the oscilloscope it is needed to take into account the influence of the input capacitance in the measurements, especially with small values of the TTCC output capacitor. This is due to that both capacitances are added, resulting in an apparent slower transition time. In this case, the output capacitor of the variable transition time circuit is 1 nF and the input capacitance of the oscilloscope is 13 pF. It is just a 1.3 % of the total value so it can be neglected.

5.8 SOT pulser + TTCC experimental outcomes

Finally, measurements of the SOT pulse generator plus the matching stage when controlled with the TTCC circuit have been carried out. A block diagram of the full system is shown in Figure 5.26.

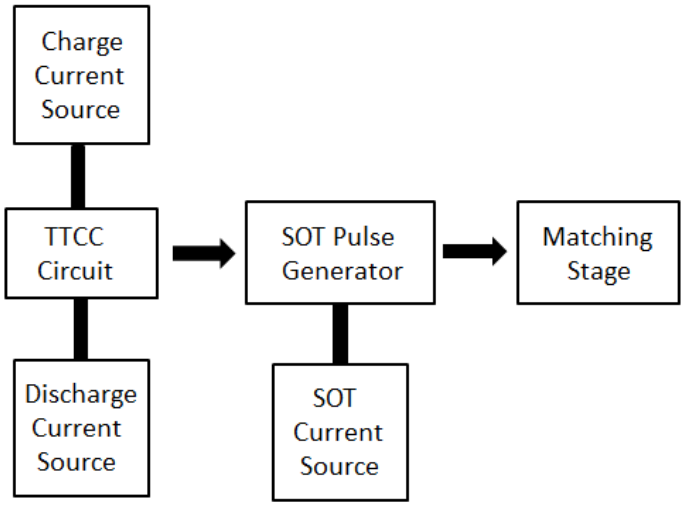

Figure 5.26 Block diagram of the SOT pulser full system

As previously remarked, some aspects have to be taken into account. First, that the load connected to the output of the TTCC must present high impedance. This is accomplished by the Mosfet gate impedance of the SOT pulse generator. Second, that the input capacitance of the SOT transistors can affect to the result as its capacitance is added to the value of the TTCC output capacitor, causing slower transition times. Finally, an matching

stage is necessary in order to connect the high impedance required by the SOT pulser to a low impedance load.

The measurements obtained by means of the oscilloscope Agilent Infiniium DSO81204B are represented in Figure 5.27. Pulse widths of 355, 180 and 115 ns have been achieved for charging / discharging currents of 10, 20 and 30 mA, respectively.

Jittter measurements have not been taken as it is not possible to cancel one of the pulses corresponding to the rise or to the fall edge. For doing so, a future improvement of this circuit has to be carried out, which allows the working of the SOT pulser current source in the desired edges.

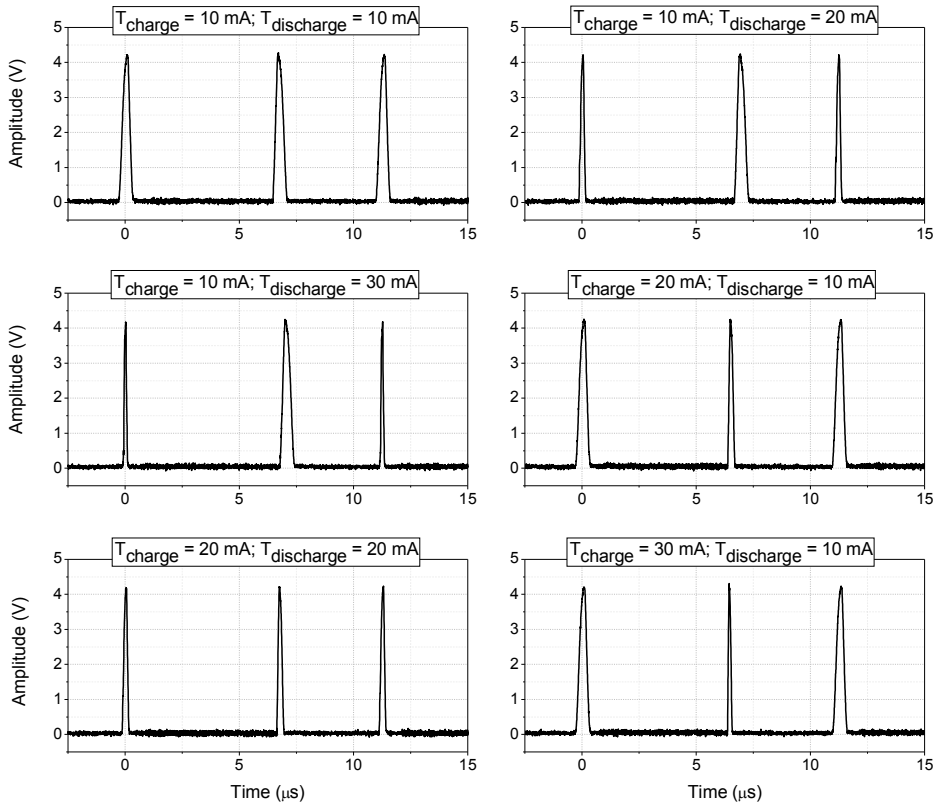

Figure 5.27 Full system output

The above results show the proper behavior when controlling the SOT pulse generator by means of the variable transition time circuit. Furthermore, the design here presented is viable for remotely controlling both the generation and the width of the pulses. The first is achieved by adding the circuitry necessary for enabling and disabling the SOT current source, so the pulses are generated when desired. It could be performed with for example just a transistor for turning on and off the current source. Regarding the control of the pulses width, it is carried out by just replacing the analog potentiometers of the variable transition time circuit for digital ones. Thus, controlling both of them it is possible to create any pulse

pattern. In conclusion, this possibility of electronic control opens a new range of applications in automation processes.

5.9 SRD and SOT pulser comparison

One of the most important advantages of the SOT with respect to the SRD pulse generator is that it is possible to control and modify the width of the pulses. In the SRD pulser it is not possible since each PCB is built with just a specific pulse width, established by the stub length.

A very important feature of the SOT pulser is its high immunity to the signal control ringing. Since the pulse is created during the middle of the control signal transition, it is not affected by the very common signal distortion produced at the beginnings and ends of the edges.

The maximum pulse repetition frequency achievable is greater in the SOT pulse generator than in the SRD pulser. This is due to the fact that the SRD-based pulse generators are limited by the charge and discharge times, and frequencies beyond around 200 MHz cannot be reached [2]. Regarding the SOT pulser, it does not suffer from this limitation. And, furthermore, two pulses are obtained per pulse of the control signal, one at the leading and another at the falling.

Another important issue is the dependence of the pulse position with temperature in SRD-based generators. Unfortunately a temperature controlled chamber was not available at the laboratory for performing an analytical test, so the variations in pulse position were proven by simply supplying the air of a fan directly to the PCB. Doing that, high changes in pulse position were observed.

Additionally, the jitter is expected to be higher in a SRD-based pulser than in the SOT pulser [2]. Nevertheless the results obtained in this thesis have been the opposite. It can be supposed that the jitter measurements in the SOT pulser have been degraded because of: a) the use of a current source based on a JFET and a potentiometer, that may probably introduce some fluctuations which in the ns range operation of the circuit become critical, and b) the use of discrete components. It is expected that using a very stable current source and an integrated circuit implementation, the jitter will be highly improved. On the other hand it may be underlined that the values of the jitter achieved with the SRD pulse generator design here developed have been quite good.

Finally, the implementation of the SOT pulser into a monolithic integrated circuit is much simpler to carry out since it is mainly by transistors and even all of the same type. On the contrary, the SRD-based pulser requires fabricating SRDs, capacitors and Schottky diodes on the same substrate, apart from the length of the stub, which involves greater difficulties.

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Chapter 6. Validation and Verification (V&V) of selected Requirements and Specifications

6.1 Framework of the V&V process

In CTA jargon, the concept "Requirement" is associated to a high level performance condition to be met, whereas the "Specifications" are lower level conditions that are identified by the telescope projects as those to be fulfilled in order to guarantee the compliance with a given requirement. The term "Validation" is used to identify compliance with a requirement, whereas "Verification" means fulfilment of a given specification. In some cases, due to limitations in the traceability processes it is not possible to guarantee the validation of a given requirement by means of the verification of a set of specifications. That would be the ideal situation. Therefore, separate compliance with both requirements and specifications is generally needed.

CTA has established a central camera testing by the Camera Test Facilities (CTF) to conduct an independent cross-check of the main performance, stability, and durability of high level requirements [1]. All CTA camera designs should go through the central CTF testing before being accepted as contribution to CTA. The validation process of the requirements for the LST was first explained in [2]. This document was one of the deliverables of the project "The Preparatory Phase for the Cherenkov Telescope Array (CTA-PP)" funded by the EU FP7 programme. It contains a description of the validation methods that must be followed to demonstrate the compliance of the telescope with all the agreed requirements. It also includes the procedures to follow in order to verify the lower level LST specifications, which are part of the requirement validation process. An upgrade of the LST V&V document was recently released [3].

The requirement validation is critical to guarantee the financial support for the construction of the entire LST array. In this chapter, a discussion of the validation of some of the most important requirements is made. The scope will be restricted to some of those requirements and related specifications where the pulse generators developed for this thesis could be used. It is not intended here to exhaustively cover all these requirements and specifications, just those where the validation is considered particularly critical and where there is a lack of available human resources to perform it. It must be pointed out that the work presented here must be harmonised with the one done by a number of other researchers, as explained in Chapter 1.

The latest available version of the LST requirements is 3.02 [4], which also includes a list of goals. Requirements in CTA define the minimal design constraints for elements to be considered part of the final array, whereas goals are characteristics of the constitutive

elements which are considered to be potentially achievable and desirable if they can be achieved without sacrificing required performance, cost, or schedule of the project [5]. The requirements are the only ones considered compulsory for the validation.

Compliance is pending in some cases as the validation of those requirements depend of elements outside the scope of LST (such as Array Trigger) or tests to be performed during the integration of the camera, for instance, or even in the field, once the first telescope is built.

Although this work is mainly focused on the LST development, it is believed that some of the results presented here are equally valid to the other CTA telescopes, since all of them must comply with the same level A requirements, which are derived to similar specifications.

LST V&V document lists a total of 112 requirements, and at present the LST project considers that 33 should be considered validated in the compliance matrix, according to [3]. This is shown in Table 6.1. Some slight discrepancies are found with the number of requirements listed in [4], due to the fact that both documents are submitted to periodic revisions.

Category	Num of Reqs.	Validated Reqs.
A-ENV	28	6
A-PERF	17	5
A-RAMS	38	1
B-LST	29	21
TOTAL	112	33

Table 6.1 Status of the Validation of the LST requirements

The agreed V&V process followed in the LST project [3] is based on five standard procedures, which are described in [6]:

- Inspection: Examination against applicable documentation.
- Analysis: use of analytical data or simulations.
- Demonstration: a qualitative exhibition of functional performance, usually accomplished with no or minimal instrumentation.
- Test: Experimental V&V under realistic conditions.
- Certification: Check against legal or industrial standards. This is the case for the V&V of parts that are outsourced, i.e, supplied by an external company.

Requirements to be validated via tests were already identified in the LST project. Validation tests are sometimes confused with development tests, which are not aimed at validating a

requirement but at demonstrating the proof of concept, feasibility or basic functionalities. These kind of tests are usually made by the prototype developers and reported in the CTA internal meetings. In this Chapter tests oriented to the formal V&V process are discussed.

6.2 The Survival Illumination Requirement

The requirement A-ENV-1430 states

"Illumination of telescope components and in particular cameras by non-calibration, artificial light sources on or near the site must not exceed 10^6 photons ns^{-1} $sr^{-1}cm^{-2}$, and must occur less than once per week for any given telescope".

This refers to conditions for the observatory site and infrastructure (shielding of neighbour roads, presence of artificial light sources, etc.). The site must guarantee that illumination of the camera never goes beyond this limit, but at the same time the camera must be able to survive to this limit. The requirement that guarantees so is A-PERF 2260, which states

"The camera must remain undamaged after illumination of any or all pixels for up to 10 seconds at an intensity of 10^6 photons ns^{-1} $sr^{-1}cm^{-2}$"

Related specifications are the following ones:

C-LST.0129, "The camera must stay undamaged under illumination of any or all pixels for up to 10 seconds at an intensity of 10^6 photons ns^{-1} $sr^{-1}cm^{-2}$, with a recurrence rate of once per week."

C-LST-CAM.0241 "The maximum DC current the HV power supply for the photosensor will be limited by design, so it will not be able to damage the sensor or associated devices in case the photosensor is illuminated continuously."

C-LST-CAM.0242 "The preamplifier board will not suffer any damage with the maximum amplitude pulses the photosensor is able to produce."

According to the LST DVD, the compliance of the requirement is considered guaranteed when these three specifications are verified. A single setup to verify simultaneously C-LST.0129 and C-LST-CAM.0242 could be used. Verifying the second specification is just reduced to check the operating conditions in the camera documentation and should be complemented (although not explicitly required) with a verification that the control SW works properly when ramping up the PMT voltages, once it is installed. The third specification will be discussed in Section 6.6.

It must be pointed out that C-LST.0129 does not specify the type of source to use in the tests. The unit corresponds to a total optical power (rather than a spectral density power) per unit of solid angle and per unit of area. Therefore one can assume that in order to validate the specification it would be necessary to check the survival of the PMTs at the exposure of two different types of light sources, one covering all the wavelengths of the PMT

and the other with a narrow bandwidth spectrum, like a laser or a LED at the wavelength were the PMT has its peak quantum efficiency (the worst case situation).

A cold white LED could also be used as a wide bandwidth source and would be recommendable for compactness. Both sources should have the same optical brightness, once integrated to the entire spectrum. If by any method it can be shown that the stress with either the wide band or narrow band source is more demanding than the stress done with the other source, accelerated tests with this last source could be skipped. However, it is believed that a wide spectrum source provides, in any case, the best simulation of the real-world accidental exposures the camera could face during nominal operation. The worst case situation could come from an accidental exposure of a car flashlight.

The specification C-LST.0129 is more demanding than A-PERF 2260 because of the mention to a recurrent exposure, 10 seconds every week. The conditions of the experiment to validate this must take into account that according to A-RAMS-0520 the camera must have a lifetime higher than 15 years.

An accelerated stress test setup can therefore be arranged by exposing a pixel to a sequence of 10 s pulses and an arbitrarily high duty cycle. If one counts a year as 52 weeks and considers a duty cycle of 0.9090% (1 s between pulses), the resulting experiment for one pixel and one light source would last 2.38 h to simulate the stress of a single pixel over the entire camera lifetime. However, measurements over a single pixel are, in general, insufficient. The random nature of the failure process must be accounted for and therefore tests over a number of pixels are needed.

Anode damage by high current densities is the most typical issue. Overexposure to light induce high interdynode currents within the photomultiplier. The electron bombardment of the dynode surfaces releases ions and when the number is too high breakdown occurs causing the photomultiplier to glow.

The photocathodes of PMTs are also very light sensitive. Their noise behaviour is negatively affected by exposure to strong light, even in the absence of bias voltage, and may take some time to recover once they are screened from light. Typically, more than half an hour could be required for recovery. One may need several hours to return to the lowest noise levels. Spiky signal traces or discoloured photocathodes both reveal irreversible damage. Therefore, care must be taken with two specific kind of damages:

a) anode damage due to overcurrent, and
b) photocatode degradation

It is important to specify the failure criteria. A slight sensitivity degradation should not be considered a failure, since it can be compensated by conveniently ramping up the bias voltage to increase the PMT gain. Hamamatsu establishes the following failure criteria to conclude that a PMT has reached the end of its life [7]:

a) Anode sensitivity variation beyond +-50%
b) Cathode sensitivity variation beyond +-25%
c) 500 times increase of the anode dark current
d) Breakdown failure symptoms like discharge, crack, anode leakage current or others.

For the verification of C-LST.0129 it must be necessary to guarantee that the degradation of the PMT sensitivity, if occurs, can be compensated by an increase of the bias voltage within the limits set in the control software.

The verification test over the entire camera, after mounted, could be done. But this solution poses high risks for the LST and also for the MST cameras: if a problem emerges with the PMTs (they do not pass the test) the entire camera should have to be dismantled. Therefore it is more advisable to do the test over a small mini-array of modules, like the cluster of three 7-pixel modules already developed by the Japanese Consortium. The LST camera is considered available when 98% of pixels are working properly [8]. Rescaling this availability to a lower number of pixels results in a number of pixels allowed to fail that are shown in Table 6.2

Modules under test	Pixels under test	98% of pixels	Pixels allowed to fail
3	21	20.58	0
6	42	41.16	0
12	84	82.32	1
24	168	164.64	3
48	336	329.28	6
96	672	658.56	13
192	1344	1317.12	26

Table 6.2 Number of pixels allowed to fail during the accelerated stress tests

A 2.38 h accelerated stress test over a single cluster of three modules should not be considered enough to guarantee the compliance for the entire camera. No pixel failures after stress over 12 modules should, in principle, be aimed for. However, by assuming that the failure process is ergodic (i.e. ensemble average equals time average), an evidence of no failures after stress tests of four times 2.38 h over a single, three module cluster should be considered equally valid.

In order to accurately relate the intensity of the light that must be applied to the photomultiplier from the optical power of the source it is necessary to develop some calculations that are shown in Appendix A.

6.3 Trigger Latency Specifications

C-LST-CAM.0425 specification states:

"The combined latency of L0 and L1 trigger will be less than 50 ns".

CTA must use a multi-level trigger scheme to prevent the recording of a large rate of random triggers from the night sky background noise [9]. At the first level (level L0), signals from individual pixels are discriminated above a threshold. These pixel-level signals are input to a second level (level L1), trigger.

The L1 trigger is used to identify concentrations of Cherenkov signals in local regions of the camera, via a sum of first-level triggers, to form a telescope-level trigger. A third, array-level trigger, is formed by combining trigger information from several telescopes. The default reaction to the telescope level trigger is the read out of the entire camera, and the trigger system must not introduce noticeable dead times. The telescope must be able to handle high trigger rates with a negligible dead time. C-LST-CAM.0422 states explicitly,

"The Camera Trigger will support rates of at least up to 100kHz".

Trigger L0 needs the information from one single module, whereas L1 involves neighbour modules. Both trigger levels are implemented in each module of the camera. While Level 0 and Level 1 subsystems are placed in the readout board itself, the subsystem required to distribute the L0 signals among neighbouring clusters is placed at a second board called "backplane" in CTA jargon, since it is connected at the backplane of the readout boards.

The verification of latency specifications should be made with a cluster of 7 PMT modules, using ns pulsed light sources. These tests must be made with a pulse generator featuring a well-known low jitter specification and the ability to send pulses of variable repetition frequency.

In order to discriminate the influence of possible issues coming from the limited bandwidth of the photomultipliers, wide enough (10 ns) pulses should be used. On the other hand, it is necessary to perform the tests within the limits of the maximum camera trigger rate, i.e. 100 kHz. Therefore the signal to be generated could follow the pulse pattern shown in Figure 6.1. Pulse pile up due to latency issues could easily be identified with this pattern without overloading the camera trigger rate capacity. The SOT pulser presented in chapter 5 would be suitable for this application since it allows controlling the generation of the pulses.

Another trigger latency specification is C-LST-CAM.0450, which states:

"The maximum delay due to the internal trigger distribution (from any cluster to the coincidence unit and back) will be less than 300 ns".

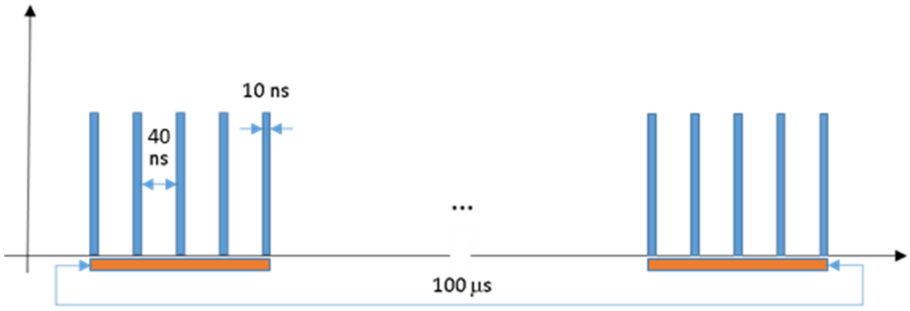

Figure 6.1 Proposed pulse burst pattern for latency tests.

The camera trigger distribution system must collect L1 triggers generated in the L1 decision circuits of each cluster, and send them to all modules in the camera. The L1 output of the trigger decision circuits is a digital pulse in LVDS standard and few tens of nanoseconds time width. The test with the signal shown in Figure 6.1 could be extended to also evaluate jitter and skew. This makes possible the simultaneous verification of C-LST-CAM.0453,

"*The inaccuracy of the clock signal distributed to any cluster, including jitter and skew, in relation to the external clock input, will be < 200 ps*".

The validation of this specification would also need a second generator to simulate the external clock. According to CTA definitions the term jitter is used to label the standard deviation of the propagation time from a given input to a given output, whereas the skew corresponds to the standard deviation of the propagation time among all possible inputs and outputs in the distribution system [10]. These tests not only demand very low jitter to the pulse generators but also to the scope. Scopes with jitter below 10 ps should be used, or alternatively a Time to Digital Converter (TDC) [11] or even a more convenient modern waveform digitizer [12].

At present the status of the verification of the trigger latency specifications is pending of systematic tests at camera level but no relevant issues are expected, since preliminary tests were recently made which basically validate the proper behaviour of the full camera trigger system [13], [14].

6.4 PMT Transit Time

Most critical issues can emerge from the lack of repeatability of the PMT transit time dispersion, and its degradation with time [15]. Transit Time Spreads in the PMTs that are going to be used in the first LST are of the order of 2.7 ns at the nominal bias voltage [16]. PMT transit time is the interval between the arrival of a light pulse at the cathode and that of the corresponding current pulse at the anode. In general, the mean transit time differs

according to where on its surface the cathode is illuminated. Transit time spread or 'jitter' is the transit-time fluctuation observed when identical light pulses strike the same part of the cathode.

PMT transit time differences are mainly due to differences in electron path lengths, but disparities in electric field strength can be relevant as well. Main contributions to this parasitic effect come from the cathode/first-dynode space, where path-length differences are greatest. At the electron multiplier path lengths are more nearly equal, does not make so important a contribution. Transit-time fluctuations in the cathode/first-dynode space have mainly two components: a chromatic one due to the spread of photoelectron initial velocities, and a geometric one due to path-length differences.

Like transit-time fluctuations, transit-time differences vary inversely as the square root of inter-electrode voltage. As it is the cathode/first-dynode space that contributes most, it is here that the most can be gained by applying the maximum permissible voltage. This is a fundamental limit for the PMT operation and it is very difficult to handle. Corrections by means of hardware require the use of pixel level analog delay lines with electronically controlled delay factors. This is difficult to implement but it is presently foreseen in the baseline design of the telescopes. On the other hand, corrections by SW would delay considerably the latency.

6.5 Noise and Bandwidth Specifications

Some of the specifications related to noise and bandwidth can also be verified with the aid of the SRD pulse generator described in Chapter 5, which is better than the SOT for this purpose due to its higher bandwidth. The relevant ones are shown in Table 6.3, all of them are particularly critical for LST, which are intended to cover the lowest energy range of the VHE spectra. The PMT is not considered part of the analog chain.

C-LST-CAM.0312	*The total noise introduced by the electronics after the PMT will be less than 0.2 phe RMS.*
C-LST-CAM.0313	*The -3dB upper cutoff frequency of the analog chain will be at 300 MHz.*
C-LST-CAM.0428	*The bandwidth of the L0 Sum Trigger will be larger than 350 MHz.*
C-LST-CAM.0432	*The signal to noise ratio (S/N) at L0 Trigger input will be larger than 4.*
C-LST-CAM.0433	*The output noise of L0 Trigger will be less than 1 phe.*

Table 6.3 Specifications related to bandwidth and noise

These tests pose no relevant difficulties, provided that the pulse generator is able to produce the signals with enough amplitude stability (low AM noise). L0 and the electronics after the PMT can be tested with the slow control board pulser, which has a design similar to the one used in MAGIC and can generate test pulses for diagnostics purposes by shaping wide pulses from a FPGA. The main challenge here is to verify the whole analog chain due to

the bandwidth limitations of the PMTs. This requires the use of pulse flashers feeding at least one cluster of three seven-pixel modules. If all the pixels verify the bandwidth specification and no repeatability issues are shown in this parameter, the specification could be considered verified.

The amplitude of the pulse corresponding to the values indicated in terms of photoelectrons can be obtained from Appendix A. The bias voltage of a PMT can be tuned for different noise gain tradeoffs. Therefore, the PMT bias during the tests must be no lower than the minimum one needed to guarantee the nominal gain of 40.000, as demanded by specification C-LST-CAM.0226. The signal to noise ratio at L0 trigger input can be measured by means of a standard single photoelectron counting procedure, that is by calculating the ratio of the mean value of the signal count rate to the fluctuation of the counted signal and noise pulses, expressed in standard deviation or root mean square.

Bandwidths can be measured with a scalar network analyser, but a dedicated test setup in the frequency domain could be too time consuming, since most of the tests on the camera electronics are done in the time domain. On the other hand, it is critical to optimise all the V&V process oriented tests in order to make them on the maximum possible amount of items within the time allocated for these tests in the global LST project schedule.

Following the basic Linear Systems Theory, the output signal of a linear system is its transfer function when the input is fed with a Dirac delta signal. Therefore, short 300 ps pulses of the prototype described in Chapter 5 can be used as Dirac deltas to visualize the L0 trigger transfer function as well as the entire analog chain transfer function in an oscilloscope. This can be done by fitting the output pulse to a Gaussian. If the standard deviation of the output pulse is σ_R, then the 3-dB bandwidth can be estimated by $B_{3dB}=0.133/\sigma_R$ [15].

6.6 The Calibration Source Specifications

In order to calibrate the camera, the absolute gain of the system has to be determined. The precise measurement of the gain of each electronic channel requires the development of a reliable calibration device, which should be able to measure the ratio of a single photoelectron to number of digital counts recorded by the system by illuminating the camera with a light source of known intensity [17].

The design concept for the calibration box of the LST's present several innovations with respect to the LED box used in MAGIC. MAGIC calibration is described in [18] and [19]. The basic component for the LST calibration device involves the generation of short pulses of UV light (350 nm) through a laser which shall be triggered and controlled by software. The intensity of the light can be adjusted by a set of filters. Uniformity of the light illuminating the LST camera is a major issue, the light must pass through a diffuser. One also may have to use

different colour light sources to quantify the differences in the quantum efficiency of the PMTs. The calibration light source should be able to generate triggers synchronous to the light pulses and also pedestal triggers for the camera.

A feedback signal to the trigger logic will also be provided in order to trigger on calibration pulses and distinguish them from real physics events. The components must be mounted inside a robust, dust-free and water-tight enclosure. High reliability as well as improved schemes for calibration and monitoring will be crucial in controlling systematic errors and exploiting the full sensitivity of the instrument. Table 6.4 shows the basic specifications for the calibration device.

By the time of writing this thesis, a prototype was already implemented by the Saha Institute using a commercial pulsed laser, which is presently under evaluation. It is however advisable to explore the options with a compact, homebrew flasher for cost reduction purposes, and then the SRD pulser described in Chapter 5 could find another possible application for CTA. The compactness would also facilitate the use of a highly rated enclosure, possibly IP 68, without significant increases in the cost.

C-LST.1001	*The width of the light pulse will be less than 2ns FWHM.*
C-LST.1002	*The wavelength of the light will be between 300 and 400 nm.*
C-LST.1003	*The Light Source will illuminate a circle of 2.4m diameter at 28 meters.*
C-LST.1004	*The Uniformity of the Light source will be < 2%.*
C-LST.1005	*The Intensity of the light source will be adjustable within a range corresponding to 0.2 to 1000 phe per photodetector.*
C-LST.1006	*The light source will be able to generate light pulses with at least three different intensities settings between 1 and 20 phe.*
C-LST.1007	*The standard deviation of the Light Pulses intensity, on a period of 30 minutes, will be less than 5%.*

Table 6.4 Specifications related to the calibration source

6.7 PMT Preamplifier Reliability and PMT survival to illumination

Although PMTs offer an internal gain, external electronic amplifiers are regularly used in PMT signal conditioning. They can have functions other than amplification, such as impedance-matching, filtering or pulse-shaping. Photomultiplier gain drops in an unpredictably way during continuous operation when the currents are high. External amplification is usually advisable under these circumstances. This makes the PMT work with lower currents and

therefore its reliability and lifetime increases noticeably. The baseline designs of both LST and MST telescope cameras include a differential amplifier after the photomultiplier.

Despite its advantages, the use of an external preamplifier demands for additional verification tests oriented to study their robustness. Charge accumulation at the amplifier input due to grounding limitations is the usual killer of a PMT amplifier. Furthermore the voltage dividers used in the internal biasing of the PMT can also destroy the PMT amplifiers, due to issues with the high voltage capacitors. Any one of this that has deteriorated over time may intermittently short and send high voltage spikes to the output, which may cause the amplifiers to fail [17].

C-LST-CAM.0242 (see Section 7.2) establishes a basic specification which is oriented to ensure the reliability of the amplifiers. To verify this specification it is necessary to pay special attention to the design of the high voltage power supply for the PMT bias, and ensure that it includes a current limiting device. Then tests must be made by exposing the PMT, connected to the amplifier, to nanosecond range light flashes with maximum intensity levels. Furthermore, the maximum level for survival conditions is set by the requirement B-LST-1010, which refers to Figure 6.2 (Figure 7 in [20]). This requirement is

B-LST-1010 *"The required fractional charge resolution for Cherenkov signals in each camera pixel under dark sky conditions is given in Figure 7. Charge measurements must be possible for 0-1000 photoelectron signals."*

Requirement B-LST-1020 defines a goal for this charge resolution in exactly the same way, but with a range of signal strengths between 0 and 2000 photoelectrons.

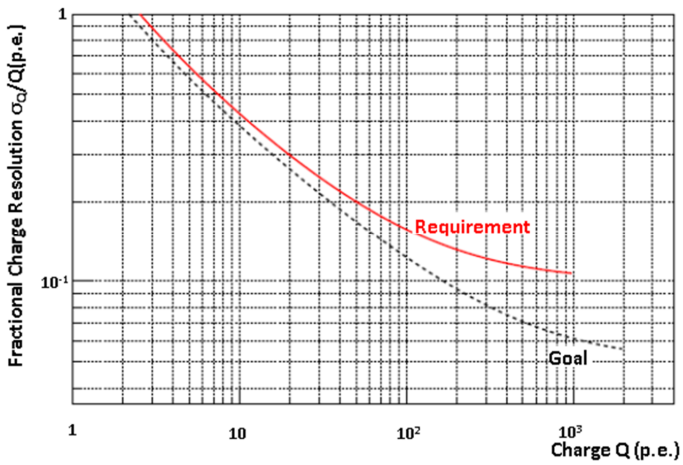

Figure 6.2 Definition of requirements for charge resolution.

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Chapter 7. Conclusions and Future Improvements

7.1 Summary and Conclusions

It is believed that this thesis has demonstrated the potential of Step Recovery Diodes (SRDs) in the development of very narrow pulse generators for a number of applications, mostly focused on the CTA project. After analyzing and designing prototypes based in different topologies, the SRD pulsers have been the most successful ones.

In addition, a new topology for ns-range pulse generation featuring electronic control of pulse width is proposed here, which has been named Signal On Transition (SOT) pulser. A summary of the major features and concluding remarks for the two main pulse generator concepts studied here follows.

7.1.1 SRD pulse generators

The pulses obtained with the SRD-based generator have more than 4 V of peak amplitude and a width of the order of one nanosecond. A state of the art width jitter in the ps range has been achieved. Additionally, the simulation of the circuit shows a high degree of agreement with the experimental results, despite the difficulty on simulating devices like the SRD or the stub in the time domain. On the other hand, with the topology presented pulse widths of less than 300 ps FWHM can be obtained.

Another feature worth to mention here is that the width of the pulse is simply controlled by just modifying the length of the stub, without the need for changing board components. This provides high versatility since the pulse generator is easily matched to the requirements of a number of different applications.

A four channel pulse generator prototype has been developed for testing the receiver boards of the MAGIC II telescope. The possibility of designing more than one independent pulse generators for multichannel feeds was shown to be impractical due to the limitations of the SRD repeatability. Nearly identical signals in these designs are needed to detect delay differences among channels and other possible anomalies of the PMT module electronics. Splitting the output of the pulse generator by means of resistive dividers and a special layout able to guarantee identical electrical lengths in all channels was shown to be a successful approach.

Due to the loss of amplitude in the fan-out stage, the four channels have been next amplified. In order to fulfill the requirements of the amplification stage such as noise figure, linearity range, wideband and high gain the amplifier 7489Z from RFMD has been chosen as it features good characteristics in those facets. Two amplifiers per channel have been

required since the 7489Z is an inverting amplifier. Additionally, a feedback resistor has been placed at the second amplifier in order to modify its operation point and achieve a greater output power.

The amplification stage has also an important role in the prevention of signal distortion. Since amplifiers feature a value of module of the scattering parameter close to zero, they impede the transmission of possible reflections produced by impedance fluctuations of the VCSELs towards the pulse generator. Additionally, some attenuators have been placed in order to avoid amplifiers saturation, which also contribute to minimize ringing.

This prototype also comprises the biasing board for the VCSELs, where a stable current source based on an OPAMP has been implemented. The design has been divided into two boards (an OPAMP per two channels) in order to use low noise amplifiers which can provide lower currents.

Finally, all the system is supplied by means of a global bias board which has been developed using resistive regulators in order to minimize noise. That has been done at expenses of a higher power consumption, what was not a critical requirement as low noise was.

A modular implementation of the complete prototype has been carried out, what lead to two main benefits: the possibility of performing independent analysis of each stage, and the ease of replacement in case of failure or improvement of a particular board.

In conclusion, a prototype of a synchronized four channel pulse generator featuring 4 V amplitude and 1.3 ns width has been implemented, composed of several stages whose design has been carefully performed in order to avoid ringing and minimize noise, and which does not widen the pulses in their transmission through the entire system.

The prototype was successfully used for testing the receiver boards of the MAGIC II telescope camera. Additionally, a 96 fanout pulse generator, based on the SRD design here presented, was developed and successfully employed for testing the readout boards of the MAGIC upgrade, which uses the DRS4 chip. Since the readout system of the CTA largest telescope (LST) is based on the same chip, this prototype was also proposed for testing the Dragon Boards (CTA readout boards).

7.1.2 SOT pulse generators

Another topology of pulse generator has been presented, based on the switching of four transistors which control the path of a current source. When the control signal changes from high to low state, or vice versa, and just in the middle of that transition, the current is driven throughout a path where a resistor has been placed. The voltage drop across that resistor generates the output pulse. Consequently pulses are created in both the raising and the

falling edges of the control signal. For that reason that pulser was been called Signal On Transition (SOT) pulse generator.

The pulse amplitude can be adjusted by means of the value of the resistance and the value of the current source. The pulse width is controlled by means of the control signal slope. That makes this generator feasible for being modified its width.

The output of the SOT circuit are inverted pulses baselined at the supply voltage. Additionally, it has to be connected to a high impedance load in order to prevent the degradation of the circuit performance. For all these reasons a matching stage has been required.

The design of this stage is composed of three OPAMPs, where high speed and low distortion have been priority facets in their selection. The two first OPAMPs act as buffers for providing high impedance and load isolation. The third one is configured as a difference amplifier for inverting the pulse and filtering the DC voltage. A different model of amplifier has been used for this one in order to have a higher power handling, necessary for achieving pulses of more than 4 V into a 50 ohms load. That has been done to the extent of a lesser input impedance, not significant in the case of the third OPAMP.

The results obtained with the matching stage show that this circuit does not widen the pulses and that there is no appreciable distortion. This is something notable since the preservation of the signal integrity is not easily guaranteed when designing matching networks from very high to low impedances, and additionally high bandwidth and relatively high amplitude signals are required.

Pulses of more than 4 V amplitude and less than 10 ns width have been achieved with the SOT pulser. The implementation carried out has been with discrete components and it is expected to reduce to a great extent the value of the minimum pulse wide achievable in an integrated circuit design.

On the other hand, a value of the pulse width jitter of 149 ps has been measured, a result much greater than expected. This is probably due to the use of current sources based on JFETs, which can cause small fluctuations affecting to the SOT generator stability. The use very stable current sources will presumably improve to a great extent this value.

Finally, a variable transition time circuit (TTCC) has been designed for controlling the width of the pulses. This circuit is based on the charge and discharge of a capacitor by means of two variable current sources. A four transistor design has been developed for keeping the current sources always active and achieving faster slopes. The transition time range can be adjusted by modifying the value of the capacitor. On the other hand, rising and falling times are independently controlled by simply changing the value of the current sources. In the design here presented it is performed by means of a potentiometer.

A TTCC with pulses of 7.5 V amplitude and transition times from 250 ns to 1.8 µs for both rise and fall edges has been carried out. With this control circuit, pulses of variable widths around the few hundred of ns are obtained. Slopes much more abrupt can be reached (and consequently minor pulse widths) by just reducing the value of the TTCC output capacitor. In the board carried out a capacitor of 1 nF has been used. For smaller values of the capacitor oscillations were observed. For that reason further analysis should be carried out in order to detect the origin of such oscillations and being able to decrease transition times. Anyway, the intention of the control circuit design was to proof the concept of the ensemble TTCC & SOT pulser, and to suggest a particular design topology.

In conclusion, it has been shown the high possibilities of the SOT pulse generator, and its versatility when combined with a variable transition time generator for leading to a variable pulse width generator. Additionally it is viable for being remotely controlled, making it suitable for automation applications.

The output pulses obtained from the pulse generators presented in this thesis (SRD and SOT pulsers) have been narrower and feature less jitter in the case of the SRD based generator. Regarding the amplitude, in both cases pulses of more than 4 V have been achieved. Nevertheless, the SOT pulser presents some properties that make from it a highly useful device, especially taken into account that with the modifications mentioned it is expected to improve the characteristics obtained to a great extent. Some of such advantages are the following:

- It is immune to the habitual ringing produced at the beginnings and ends of control signal edges, since the pulse is originated in the middle of the transitions.

- The width of the pulses is easily controllable by just varying the control signal slope, so the same PCB can provide a large range of widths which will depend on the degree of slope variability. This feature provides high versatility to the pulse generator and it is an important advantage with respect to the SRD pulser which is manufactured for a specific pulse width.

- The maximum pulse repetition frequency achievable is greater in the SOT generator than in the SRD pulser since it is not limited by the charge and discharge times required in the SRD generator.

- The pulse generation is controllable by activating/deactivating the SOT current source, being able to produce pulses just when required. The combination of this property and previous one make this generator ideal for being used in applications where high repetition frequency rates and discontinuous pulse generation are required, as for example in the burst pattern proposed for trigger latency tests.

- Finally, SOT pulser design is highly appropriated for an integrated circuit implementation, since it is essentially composed by transistors. On the other hand, the SRD pulse generator presents the inconvenient of the length of the stub, apart from necessity of fabricating different types of devices (SRD, Schottky diodes and capacitors).

7.2 Potential of the developments presented in this thesis

Besides the applications already demonstrated with the prototypes presented here, it is believed that further uses can be found for them. The verification and validation (V&V) process in CTA is presently giving its first steps. Several critical requirements and specifications have been described here, with (V&V) tests needing multichannel nanosecond range pulsers with a high peak amplitude and very low jitter, as those presented in this thesis.

A number of groups devoted to the development of electronics for the cameras of all CTA telescopes, as well as those groups involved in the management of the quality control and RAMS validation, might also take benefit of the technologies proposed here. This thesis presents designs with fabrication costs in the range of tens of Euros which provide pulsed signals that are equivalent to instruments with costs in excess of 4000 Euros. This was made possible by sacrifying a number of general purpose functionalities with marginal use for the specific applications described here. The benefits besides the cost, are the compactness, the possibility of feeding multiple channels with nearly identical shapes and delays, and the knowledge gain. In addition, once the technology has been learned and optimized, the miniaturization at chip level becomes possible.

7.3 Future improvements

There are several possibilities that could improve the behavior and characteristics of the pulse generators presented in this thesis. Some proposals are described below.

1. To study the influence of temperature on the pulse shape and jitter, with the aid of a temperature controlled chamber.
2. To study procedures to electronically control the width of the SRD prototypes.
3. To develop an ASIC for the SOT pulse generator, which is expected to reduce considerably the width of the pulses.
4. To develop circuitry for activating / deactivating the current source of the SOT pulser in order to control the generation of the pulses and to create custom pulse patterns.
5. To improve the stability of the current source in the SOT pulse generator, with the aim of improving the jitter.
6. To perform further tests of the TTCC here presented with stepper slopes, in order to prevent pulse distortion and ringing. In this case, an integrated circuit implementation is again expected to noticeably improve the transition times obtained.

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APPENDIX A. Photons and photoelectrons in wide band light sources

This appendix is devoted to discuss the mathematical framework for the estimation of the expected response of a photodetector to the light generated by a source, this last one being expressed in terms of the number of photons per nanosecond per unit of solid angle and per unit of area. The quantities that mainly affect the photodetector response are the total emitted light from the source and the angular spread of the emission with respect to the source optical axis. The procedure to convert the incident light on the photodetector into photoelectrons, and therefore into a current, will also be presented here. Without any loss of generality it will assumed that the source is a LED.

A.1 Mathematical foundations

The relationship between the number of photons and the photoelectrons provided by a PMT can be roughly estimated in simple terms if the source is monochromatic. We use the Einstein relationship: E = hc/λ, where h is the Planck constant and c is the speed of light, to calculate the energy of one photon at this wavelength. If the energy of the source is known, the number of photons is estimated by dividing this energy by E and from them the photoelectrons are usually estimated.

Let us consider now an arbitrarily wide bandwidth source. We will first concentrate on the angular spread of the emitted light. In this step of the calculation we find how much of the emitted light of the LED finally reaches the detector. A spherical reference system is established centered on the LED, with the z axis aligned with the optical axis of the LED. It can be reasonably assumed that the differential emission depends only on the polar angle θ, defined from the LED optical axis. In this way, the differential energy emitted in a dt time, and in a solid angle $d\Omega$ is

$$dE = I_d(\theta) d\Omega dt \qquad (A.1)$$

where $I_d(\theta)$ is the angular light intensity distribution. In principle, such formula should receive a monochromatic treatment, but it can be safely assumed that the angular spread does not depend on the wavelength of the emitted light since there is no diffraction implied and the chromatic aberration of the dome is negligible. Thus, it will be assumed that the angular propagation factor is the same whatever the color band of the emission is. Using Eq. (A.1), the light intensity incident on the photodetector can be expressed in this way,

$$I_{inc} = 2\pi \int_0^{\theta_d} I_d(\theta) \cdot sin\theta \cdot d\theta \qquad (A.2)$$

where θ_d is the zenith angle corresponding to the solid angle subtended by the photodetector. Following that previous definition, we can express the total light emitted by the LED as

$$I_T = 2\pi \int_0^{\theta_T} I_d(\theta) \cdot sin\theta \cdot d\theta \qquad (A.3)$$

where θ_T is the zenith angle corresponding to the solid angle of emission of the LED. This angle is usually provided by the manufacturer.

A common approximation is to suppose that $I_d(\theta) \approx constant$. In this way, the ratio between the incident light and the total emitted light can be calculated as:

$$\frac{I_{inc}}{I_T} \approx \frac{\int_0^{\theta_d} 2\pi \cdot sin\theta \cdot d\theta}{\int_0^{\theta_T} 2\pi \cdot sin\theta \cdot d\theta} = \frac{\Omega_d}{\Omega_T} \qquad (A.4)$$

That is, the ratio of intensities is the same as the ratio between the solid angles. Once the measurements are made, it will become clear that the assumption of constant intensity over the zenith angle is only an approximation, due to a not uniform emitting region of the LED. Thus, the accuracy of Eq. (A.4) can be improved. The difference between the calculated ratios of luminosity and the ratio of solid angles (a small difference, but a very significant one at small solid angles) can be used as an indicator of the precision of our method, compared to more usual calculations.

A problem that arises when using more precise formulas is that absolute data are needed. Nevertheless, by using normalized functions, that need can be eliminated. This is due to the fact that our experimental target is a ratio between intensities, a dimensionless number by its own nature. The ratio of the incident light by the total emitted light is given by:

$$\frac{I_{inc}}{I_T} = \frac{\int_0^{\theta_d} I_d(\theta) \cdot sin\theta \cdot d\theta}{\int_0^{\theta_T} I_d(\theta) \cdot sin\theta \cdot d\theta} \qquad (A.5)$$

A new flux function can be defined in this way

$$F(\theta) = K \cdot I_d(\theta) \qquad (A.6)$$

where K is a constant normalization factor calculated in order that the integration of F(θ) over the solid angle of emission of the LED is 1,

$$2\pi \cdot \int_0^{\phi_T} F(\theta) \cdot sin\theta \cdot d\theta = 1 \qquad (A.7)$$

$$K = \frac{1}{2\pi \cdot \int_0^{\theta_T} I_d(\theta) \cdot sin\theta \cdot d\theta} \qquad (A.8)$$

Thus, Eq. (A.5) can be simplified as

$$\boxed{\frac{I_{inc}}{I_T} = 2\pi \int_0^{\theta_d} F(\theta) \cdot sin\theta \cdot d\theta \leq 1} \qquad (A.9)$$

In case that the angular spread is not azimuthally symmetrical, as was supposed before, these measurements should be done on a few transversal axes, and get a mean value of such F(θ) curves. In practice, the worst case scenario implies just measuring in two perpendicular axes.

In this way, if we can get a normalized function proportional to $I_d(\theta)$, it can be used to calculate the ratio of intensities, with no need for absolute data.

A.2 Worked Example

In order to illustrate these calculations, measurements have been made with a LED model Kingbright L53MBC and an IR filtered photodiode VTB8440B. The measuring device is a high sensitivity photodiode, especially sensitive to the blue wavelength. The LED is biased using a voltage source, and the total tension will be measured by the source's own voltmeter. The forward current in the LED is derived by measuring the tension in a bias resistance of 330 Ω placed in series with the LED. As for the photodiode, variations in the incident light change the output voltage V_{phd}, which is measured through the multimeter.

It must be pointed out that in this section the quantum efficiency will be used in the calculations in order to take benefit from the manufacturer's datasheet. However, this parameter is not the best one to make accurate estimations of light to photoelectron conversion balances. The photon detection efficiency might be a better parameter for these studies. For instance, in PMTs the PDE is sensitive to collection efficiency issues in the PMT front end and also to backscatter losses. However, this parameter was not provided by the manufacturers of the photodetectors used in this study.

The characterization of the LED is done in the continuous range. The photodiode has an active area of 2x3 mm, and is set at half a meter from the LED, which means that we can safely assume that the light intensity is uniform across the detector area.

The LED is mounted on a standard goniometric base that can be rotated around the axis perpendicular to the plane where the LED and the photodiode are located. The angle between the LED optical axis and the photodiode axis defined the zenith angle of the incident light.

A calibration curve that relates the power of the incident light with the tension in the photodiode was then obtained with the LED at a 0 degrees zenith angle, for different bias voltages. This shows where is the saturation level.

Once the output voltage of the photodiode versus zenith angle has been recorded, each voltage value at θ degrees will be related to a corresponding emitted power at zero degrees. The ratio of actual power being emitted by the LED to the corresponding power at zero degrees of the response indicates the ratio of the incident intensity of the light at zero degrees to the intensity at the angle we are measuring. Therefore, we obtain a distribution of relative intensities versus angles that is proportional to the angular light intensity distribution $I_d(\theta)$.

The advantage of this method is that the quantum efficiency of the detector and other absolute quantities are not needed in order to get precise measurements. Calculating K through (A.8), the distribution function can be normalized, and so $F(\theta)$ is obtained. As the distribution is not exactly the same at both sides of the zero degrees point, an averaged value must be used for the calculations.

Let us now estimate the light from the LED. To do so we use the relation between the forward current and the relative luminosity of the LED provided in the technical datasheets. As the current values of the LED are being registered, it is straightforward to get the corresponding total emitted intensity.

Once the total emission (in watts) is multiplied by (A.9), the result is the incident intensity I_{phd} of light into the photodetector. In order to calculate the number of incident photons, the emission spectrum $N(\lambda)$ of the LED is needed. The light emitted by the LED in the wavelength interval $\lambda \pm d\lambda$ is given by:

$$P = kN(\lambda)d\lambda \qquad (A.10)$$

The emission spectrum is usually normalized so that $N(\lambda_{peak}) = 1$ so its highest density value is equal to 1 (or some other arbitrary unit). Then, an unknown k value is needed. The emitted power in a wavelength interval (λ_i, λ_f) is

$$P = k\int_{\lambda_i}^{\lambda_f} N(\lambda)d\lambda \equiv P(I_{LED}) \qquad (A.11)$$

If the $N(\lambda)$ curve is digitalized, its integral can be found, and the k value can be automatically found, if the $P(I_{LED})$ emitted power, a function of the current intensity of the LED, is well known.

$$k = \frac{P(I_{LED})}{\int_{\lambda_i}^{\lambda_f} N(\lambda)d\lambda} \qquad (A.12)$$

Thus, the number of photons per second within $\lambda \pm d\lambda$ incidents onto the photodetector will be:

$$n_\gamma(\lambda) = \omega \frac{k \cdot N(\lambda) d\lambda}{hc/\lambda}, \quad \omega \equiv \frac{I_{inc}}{I_T} \tag{A.13}$$

And the number of primary photoelectrons generated is calculated by multiplying the number of photons by the photodetector quantum efficiency $QE(\lambda)$

$$n_{phe}(\lambda) = \omega \frac{k \cdot N(\lambda) QE(\lambda) d\lambda}{hc/\lambda} \tag{A.14}$$

Then, integrating in the wavelength interval (λ_i, λ_f), and substituting the k value, the final expression of the number of primary photoelectrons will be:

$$\boxed{n_{phe} = \frac{\omega}{hc} \frac{P(I_{LED})}{\int_{\lambda_i}^{\lambda_f} N(\lambda) d\lambda} \int_{\lambda_i}^{\lambda_f} N(\lambda) QE(\lambda) \lambda d\lambda} \tag{A.15}$$

The modeling of the LED emission described above was applied to determine the number of photoelectrons generated by a photomultiplier (PMT) in response to a short light pulse. As for the PMT we have made use of a six dynode EMI 9116, with a typical quantum efficiency (QE) of 25 % and the peak response in the UV wavelengths. For the LED, we have used a high luminous L7113PBC from Kingbright, with a maximum light intensity of 1 cd at a peak wavelength, λ_{LED} , of 468 nm (for a forward current I_f=20 mA). The LED was fed with 10 ns pulses. Figure A1b-d summarizes the results obtained.

We will apply now Eq. (A.15) to estimate the number of photoelectrons, thus a calibrated PMT is used in the setup. We have to insert into Eq. (A.15) the emission spectrum of the LED, the angular distribution of the emitted light and the quantum efficiency of the PMT as a function of the incident light wavelength. The LED emission spectrum and the PMT QE are assumed to be known. The spatial distribution of the light emitted by the L7113 LED (for a fixed forward current) was directly measured using the VTB8440B photodiode placed at 35 cm from the LED and at the same height. From this measurement, we derived the normalized function *F(θ)* . The integration angle θ_d of Eq.(A.9) is determined by the radius of the detector, R, and the distance d to the LED. In our case, R=11mm and d=300mm, thus θ_d=1.8° .

Since a calibrated lamp for photometric measurements was not available, the power emitted by the LED for a given forward current at the peak wavelength, P(λ_{peak}), must be derived from the curve of the relative radiative power as a function of If given by the manufacturer. For the LED pulse showed in Fig. A1d, we have V_f =2.72V (peak value), which corresponds to an I_f =1.4 mA, according to the IV curve of the LED manufacturer. Given the

good linearity of the LED at these currents, this corresponds to an emitted intensity $P(\lambda_{peak}, I_f=1.4mA)=(1.4/20)\cdot P(\lambda_{peak}, I_f=20mA)= 0.07\cdot 1$ cd $\approx 10^{-4}$ W/sr.

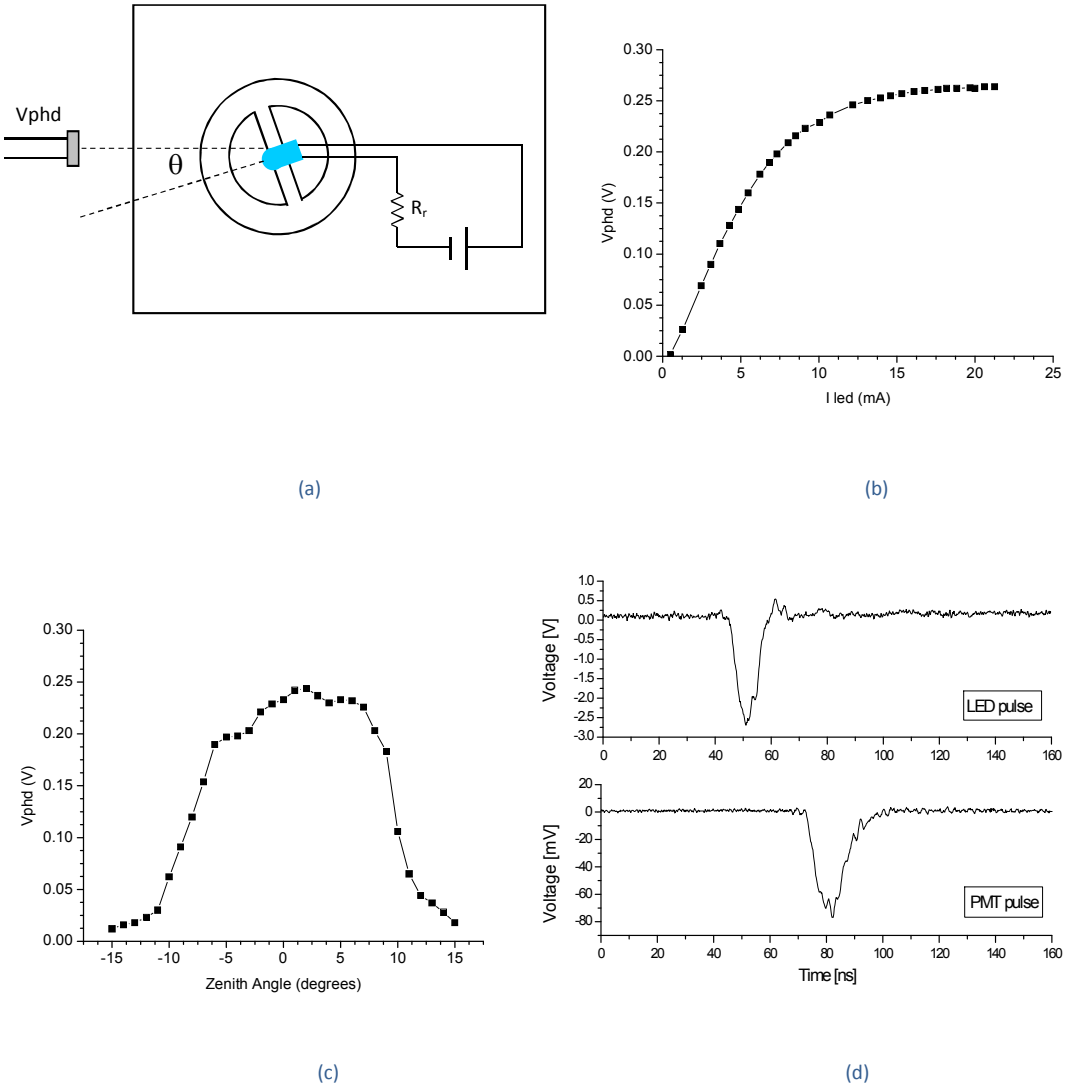

Figure A.1 Experimental setup (a), photodiode response (b), LED radiation diagram (c) and pulse waveforms (d).

Inserting in Eq. (A.15) all the parameters needed and integrating $F(\theta)$ up to θ_d , we get for the light pulse generated and for the PMT ET9116 placed at 30 cm from the LED, a photoelectrons luminosity $n=7.47\cdot 10^{11}$ phe/s. Since the gain of the PMT, according to the polarization applied, is $G=10^4$, the number of photelectrons emitted is converted to an anode pulse current $I_a=1.19$ mA. For a load resistance R=50 Ω (input oscilloscope impedance) we get an estimated anode voltage drop $V_{pulse} \approx 60$ mV. The measured pulse is 76 mV.

APPENDIX B. Toy Monte Carlo Simulation of Voltage Fluctuations in the Time Domain

B.1 Motivation

One of the major concerns to be addressed in the design of nanosecond pulse generators for quality control is to ensure that the noise injected to the devices under test is low enough and can accurately be quantified. Since the major power noise sources are proportional to the bandwidth, as the pulse width decreases the bandwidth of the system needed to detect or process it increases, and therefore the system sensitivity decreases.

Buffer amplifiers and noise pads are typically used after the pulse generators to avoid mismatches and ringing. In order to accurately distinguish between the noise generated by the circuit under test and the one injected by the measurement system (i.e. the combination of the pulse generator, a buffer amplifier and/or a dissipative pad) a software tool based on the Monte Carlo method has been developed by the UCM-ELEC group, which is able to provide a full time domain description of the detected pulse signals polluted with noise. The tool developed is applied to simulate the influence of the noise generated by amplifiers and pads on the generated pulse.

B.2 Theoretical framework

The noise factor F of a two port network is described by

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{N_a + GN_i}{GN_i} \qquad (B.1)$$

Where G is the system gain and S_i / N_i , S_o / N_o are the input and output signal to noise ratios, respectively. The equivalent noise temperature, T_e represents the temperature at the input of the network that would generate a noise equivalent to the one generated by the amplifier

$$T_e = T_0(F - 1) \qquad (B.2)$$

Major noise sources, like thermal or shot noise, have a white spectrum at room temperatures up to THz frequencies, as well as a Gaussian probability density function. Therefore, the standard deviation of the probability density function of the normalized voltage noise generated by the amplifier is given by:

$$\sigma = \sqrt{\frac{kT_eBG}{2}} \qquad (B.3)$$

It must be taken into account that this factor is applicable to the case of a normalized load resistance. For an arbitrary input load R_L, the standard deviation must be multiplied by the square root of this resistance.

The simulation of the output signal polluted by the amplifier noise has been made by means of the Monte Carlo method, where the key input data are the noise factor and the scattering (S) parameters of the buffer amplifier, matching pad or the cascade combination of both. These data are usually provided by the manufacturers, or can easily be measured in a laboratory with a microwave noise meter and a vectorial network analyzer. In the case of a passive matching pad, the theoretical noise temperature can accurately be calculated, as indicated in Section B.4 of this appendix.

The design of a suitable preamplifier for the photodetectors must take into account other parameters (stability, reflection losses, pulse ringing, etc.) to achieve a feasible prototype. Therefore, the simulation has been integrated in a general purpose software tool which provides a full description of the output signals.

The voltage noise is simulated by adding to the ideal noiseless pulse a noise voltage which is obtained by generating Gaussian random numbers with the standard deviation given by (B.3). The generation of these numbers can be obtained by using standard techniques. In MATLAB, for instance, the command “randn” generates pseudorandom numbers with a gaussian distribution having a standard deviation equal to one.

Following the basic theory of random variables, a vector of random numbers with an arbitrary standard deviation σ can be obtained by multiplying by σ the numbers given by “randn” command. In Excel the inverse transform method can be used via the command “NORM.INV(RAND(), 0, σ)” for the same purpose, being RAND() the command that generates numbers uniformly distributed between 0 and 1. Therefore, the major issue to address is the estimation of the standard deviations from the electrical parameters that are typically known. The examples described below illustrate how to do this.

B.3 Influence of the bandwidth and buffer amplifier

Figure B.1 shows the dependence of the amplifier output pulse noise with the bandwidth. An ideal filter with the specified bandwidth has been used in the simulations. High bandwidth increments the system noise, while low bandwidth can distort the pulse shape. In the simulations, an amplifier with a gain of 10 dB and a noise figure of 3 dB has been used. The noiseless pulse at the input of the buffer is represented in this figure by a black line. Since the scale has been optimised to better visualize the noise voltage, the shape at the input is not distinguished. A Gaussian pulse was however used and can be clearly observed at the amplifier output. No distortion effects are introduced by the amplifier since the S parameters used for this simulation assume an ideal inverting amplifier with a linear phase and flat gain. The voltages are normalised to 1 Ohm. For an input load resistance of 50 Ohm, the values must be rescaled by a factor of 7.07. Therefore for this particular case one can reasonably predict that the voltage fluctuations with this standard load will clearly be observed for test pulses below 1-10 mV.

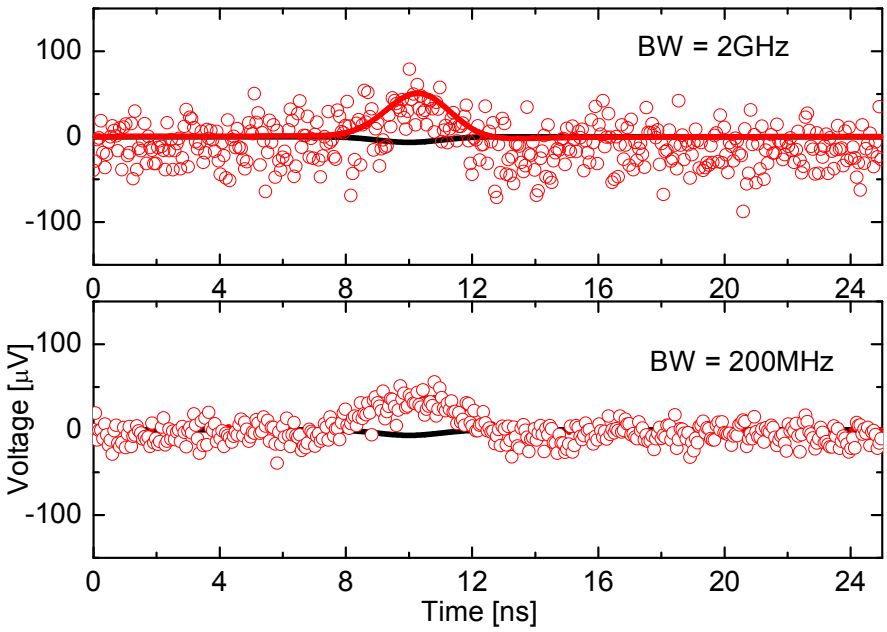

Figure B.1 Dependence of the pulse noise with the bandwidth. Black line: input signal. Red line: ideal output signal for a noiseless amplifier. Red circles: real output.

Figure B.2 shows the dependence of the output pulse noise with the noise figure of the amplifier. The noise figure is assumed to be variable while the scattering parameters are kept constant, with the same values of the previous simulation. The bandwidth used in the simulations is 3 GHz.

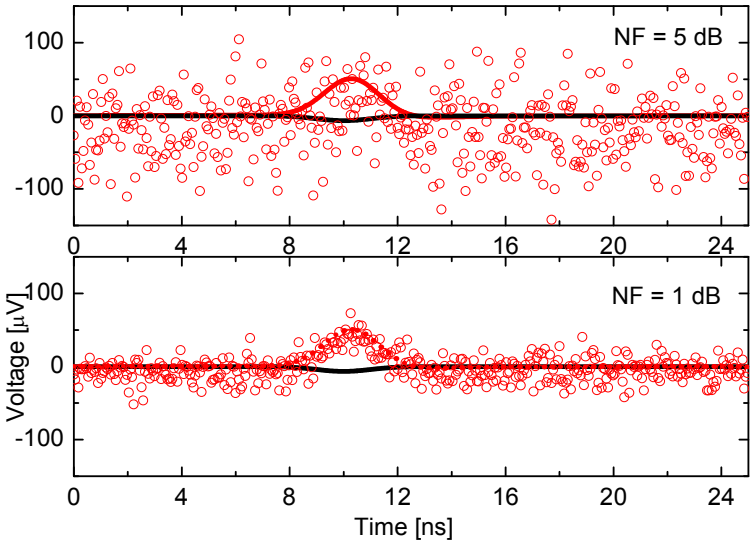

Figure B.2 Dependence of the pulse noise with amplifier's noise figure. Black line: input signal. Red line: ideal output signal for a noiseless amplifier. Red circles: real output.

B.4 Effects of a dissipative matching pad

Pulse ringing can suitably be reduced by the use of a dissipative pad. It can be implemented with a T resistive network or with a coaxial discrete component, which has almost the same size of a connector adapter. With the pad one relaxes the demands for low S_{22} in the buffer amplifier design and there is no loss in bandwidth. In addition, the amplitude of pulse echoes is attenuated and the stability improved. However, it is necessary to know what price must be paid in terms of sensitivity.

A dissipative pad with an attenuation factor A reduces the voltage standing wave ratio (VSWR) in a fairly broad band of frequencies. As a result, the ratio true-pulse-peak-voltage / secondary-pulse-peak-voltage increases by a factor of $A^{1/2}$. Following the relationship betweem VSWR and the reflection coefficient modulus, it can be seen that the final VSWR (VSWR') is related to the original one (VSWR) by

$$VSWR' = \frac{VSWR(A+1)+A-1}{VSWR(A-1)+A+1} \qquad (B.4)$$

The equivalent temperature $T_{e,pad}$ of a dissipative pad with attenuation factor *A* is

$$T_{e,pad} = (A-1)T \qquad (B.5)$$

where *T* is the physical temperature of the pad. If this pad is connected to an amplifier input with gain *G* and equivalent temperature $T_{e,amp}$ the overall equivalent noise temperature is given by the Friis equation,

$$T_{e,total} = T_{e,pad} + AT_{e,amp} \qquad (B.6)$$

Figure B.3 shows a simulation that illustrates how the pad increases the noise of a pulse with a ringing effect produced by a mismatch between the buffer amplifier input and the pulse generator. The pad inserted between the amplifier and the generator mitigates the ringing at the expense of increasing the noise.

The new probability density function of the voltage noise generated by the amplifier and the pad is therefore

$$\sigma' = \sqrt{\frac{kBT[T(A-1) + AT_{e,amp}}{2A}} \qquad (B.7)$$

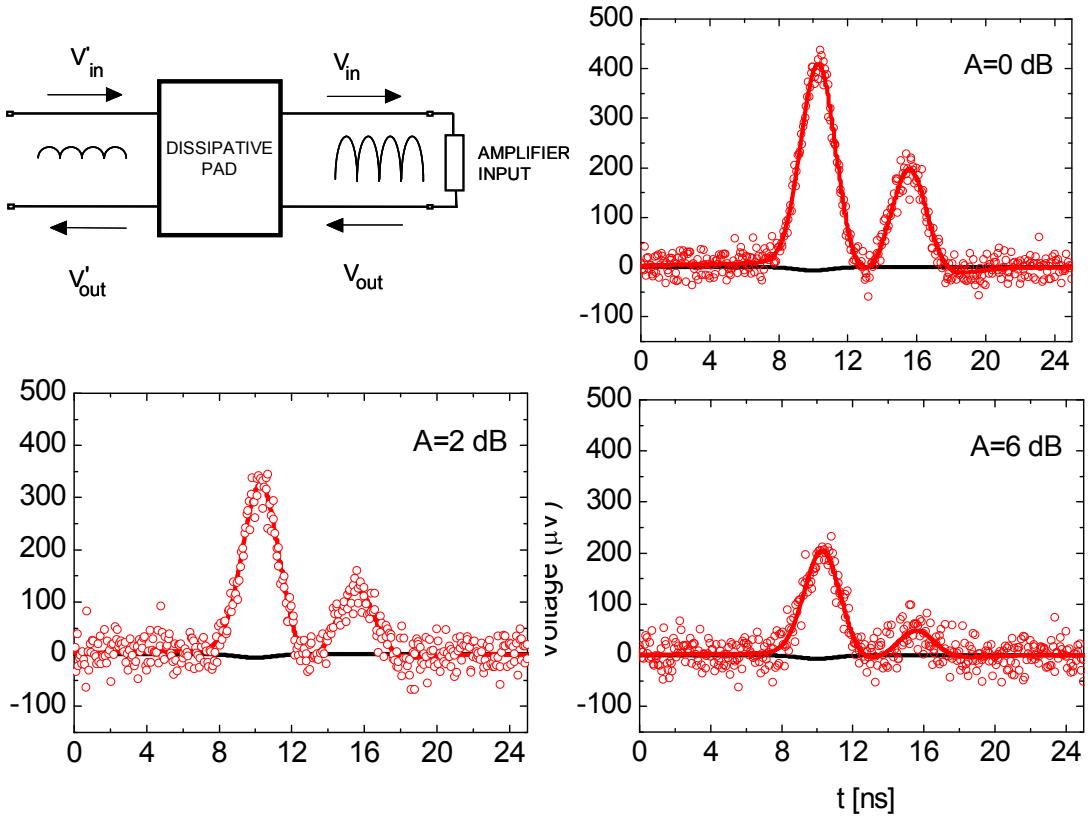

Figure B.3 Dependence of the amplifier output pulse on the attenuation factor of the dissipative pad. Mismatches between the photodetector and the amplifier are considered. The bandwidth is 3 GHz and the amplifier noise figure is 3 dB.

Figure B.4 shows an example of the dependence of both pulse and noise amplitude with the variation of the attenuation *A*. It is noticeable that the increment of σ with A is very weak. The bandwidth (BW) is 3 GHz and the amplifier noise figure (NF) is 3 dB. This NF corresponds to the one obtained for the designed amplifier. The BW has intentionally been chosen as the maximum one for practical sub ns pulse detection, in order to test an almost worst-case situation for the pad.

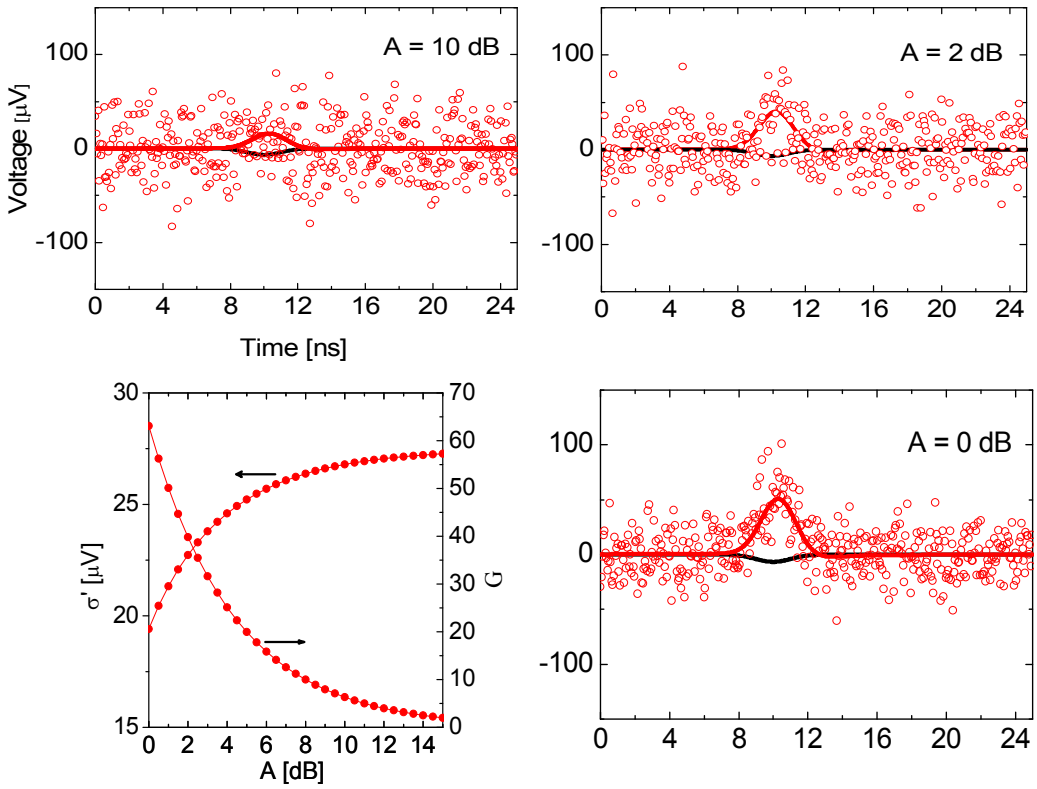

Figure B.4 Dependence of the amplifier output pulse on the pad attenuation. The lower graph on the left shows the dependence of σ' and overall gain on the attenuation factor.

B.5 Concluding remarks

The simulations presented in this appendix illustrate how a full time domain representation of the signals that would be measured for a given pulsed output can be reproduced, once the amplifier S parameters and noise figure are known. This representation has enabled us to have an accurate knowledge of what can be expected in terms of pixel sensitivity and amplifier bandwidth.

It can also be concluded that it is not possible to obtain optimum figures of merit for a suitable preamplifier if one does not have a previous knowledge of the minimum signal

levels that the pulse generator can generate with a reasonable signal to noise ratio. In our simulations we have intentionally used noiseless input pulses in order to better visualize the contributions of the amplifier and pad noise. However, if the pulser produces noise with standard deviations comparable to the ones calculated in this work, careful attention must be paid in selecting the proper gain and bandwidth of the preamplifier, since this device will amplify the input noise as well.

In the simulations presented here we have considered input data typical of the photodetectors that will be used in the CTA cameras, and bandwidths, gain and noise figures that have been obtained in the different preamplifier prototypes that have been designed. In addition the detailed knowledge of the expected noise that one should obtain at the preamplifier output can also help to identify and eliminate other sources of parasitic signals once the camera is mounted. Furthermore, the models in which these simulations are based have a wider range of applications and could also be helpful for noise diagnosis in other fields.

APPENDIX C. Low bandwidth pulse generator based on a Schmitt Trigger inverter adjustment

Along this thesis the primary low-bandwidth pulses used in the prototypes developed have been created by means of the pulse generator of Figure C.1. This circuit bases its operation in the charge and discharge of the capacitor placed at the input of the Schmitt Trigger inverter. Assuming the inverter output is initially at high level, the capacitor is being charged through resistor R_2. Once the positive threshold voltage (V_{t+}) is reached, the inverter changes to low state. Consequently, the capacitor starts to discharge through R_1 and R_2. When the voltage across the capacitor reaches this time the negative threshold voltage (V_{t-}), the output of the inverter switches to its high level, and thus cyclically. It can be noticed that the maximum and minimum voltages across the capacitor correspond to the positive and negative inverter threshold voltages.

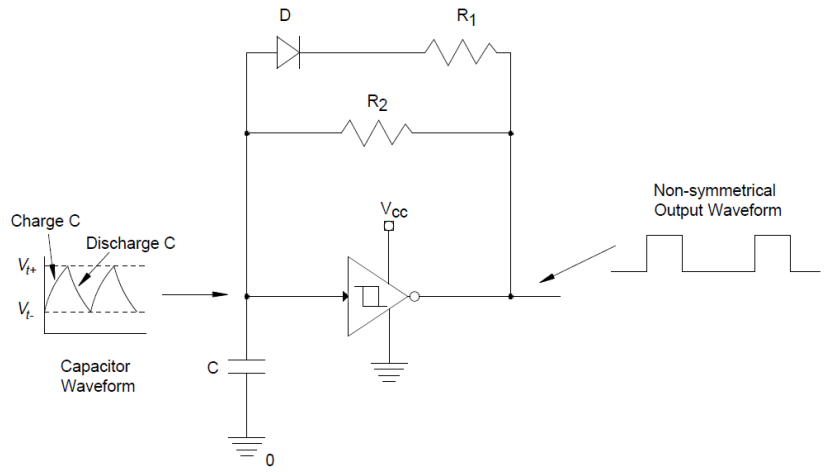

Figure C.1 Pulse generator based on a Schmitt Trigger inverter schematic

The frequency and duty cycle of the output can be controlled by modifying the value of the resistors. However, it is needed to take into account the following remarks:

- The value of the resistance is not the same for the charge and the discharge paths.

- The values of the threshold voltages are not symmetric in the Schmitt Trigger inverter.

In order to perform an accurate adjustment it is required to analyze the charge and discharge times.

Charge Time

When the inverter output is at high level (V_{OH}), the capacitor is charged through R_2, so

$$V_{OH} = V_{R_{EQ}} + V_C(t) \tag{C.1}$$

where $R_{EQ} = R_2$. Substituting $i(t) = dq(t)/dt$ and $dq(t) = CdV_C(t)$ yields,

$$V_{OH} = R_{EQ}C\frac{dV_C(t)}{dt} + V_C(t) \tag{C.2}$$

Separating variables and integrating between the initial (t_0) and final (t_f) times,

$$R_{EQ}C\int_{V_C(t_0)}^{V_C(t_f)} \frac{dV_C(t)}{V_{OH} - V_C(t)} = \int_{t_0}^{t_f} dt \tag{C.3}$$

The left part of the equation (C.3) is an immediate integral whose solution is given by $\int \frac{f'(x)}{f(x)}dx = ln|f(x)| + C$. Thus, solving (C.3) for t_{charge} yields,

$$t_{charge} = t_f - t_0 = -R_{EQ}C\left[\ln\left(V_{OH} - V_C(t)\right)\right]_{V_C(t_0)}^{V_C(t_f)} = -R_{EQ}Cln\left(\frac{V_{OH} - V_C(t_f)}{V_{OH} - V_C(t_0)}\right) \tag{C.4}$$

Discharge Time

When the inverter output is at low level (V_{OL}), the capacitor discharges through the resistances R_1 and R_2. Thus,

$$V_{OL} = V_{R_{EQ}} + V_C(t) \tag{C.5}$$

where now $R_{EQ} = R_{\|} = R_1R_2/(R_1{+}R_2)$. Proceeding in a similar way as before and solving for $t_{discharge}$ it is obtained,

$$t_{discharge} = -R_{EQ}Cln\left(\frac{V_{OL} - V_C(t_f)}{V_{OL} - V_C(t_0)}\right) \tag{C.6}$$

A summary of charge and discharge times is shown in Table C.1

	Charge time	Discharge time
Equation	$-R_{EQ}Cln\left(\frac{V_{OH} - V_C(t_f)}{V_{OH} - V_C(t_0)}\right)$	$-R_{EQ}Cln\left(\frac{V_{OL} - V_C(t_f)}{V_{OL} - V_C(t_0)}\right)$
R_{EQ}	R_2	$\frac{R_1R_2}{R_1+R_2}$
$V_C(t_0)$	V_{t-}	V_{t+}
$V_C(t_f)$	V_{t+}	V_{t-}

Table C.1 Charge and discharge times of a pulse generator based on a Schmitt Trigger inverter

APPENDIX D. List of Components

4-CHANNEL SRD PULSE GENERATOR				
Component	**Qty.**	**Package**	**Retailer / Manufacturer**	**Code**
Pulse Generator				
Inverter 74AC14SC	1	SOIC-14	Farnell	1014141
Resistor 100 Ohm	2	SMD 0805	Amidata	347-9780
Resistor 300 kOhm	1	SMD 1206	Farnell	1100256
Resistor 1.5 MOhm	1	SMD 0805	Farnell	9238018
Capacitor 47 pF	1	SMD 0805	Farnell	499160
Capacitor 10 uF	2	SMD 1210	Amidata	515-8485
Diode 1N4148 (Fairchild)	1	DO-35	Farnell	9843680
Schottky Diode BAT17 (NXP)	2	SOT-23	Farnell	1081187
Step Recovery Diode SMMD832	2	SOD-323	MCE Metelics	SMMD832
Pulse Division				
Resistor 30 Ohm	5	SMD 0805	Farnell	6183151
Pulse Amplification				
Resistor 15 Ohm	8	SMD 0805	Amidata	347-9673
Resistor 560 Ohm	4	SMD 0805	Amidata	347-9881
Inductor 10 uH	8	SMD 1210	Amidata	548-2687
Capacitor 1 uF	12	SMD 0805	Farnell	9227792
Capacitor 1 nF	4	SMD 0805	Amidata	237-6977
Attenuator 6 dB, DC-2500 MHz	4	SOT-143	Minicircuits	Lat-6+
MMIC Amplifier SGA7489Z	8	SOT-89	RFMD	SGA-7489Z
VCSEL Biasing				
OPAMP OP27EPZ (Analog Devices)	2	DIP-8	Amidata	522-8736
Resistor 1 MOhm	8	SMD 1206	Farnell	513090
Resistor 560 Ohm	6	SMD 1206	Farnell	9236805
Inductor 68 nH	4	SMD 0805	Farnell	1198402
Inductor 100 uH	4	SMD 1812	Amidata	367-4424
DC Regulation				
Regulator LM317TG	4	T0-220	Farnell	1130736
Trimmer 1 kOhm	3	THD Vert. Adjust	Farnell	9608591
Trimmer 5 kOhm	1	THD Vert. Adjust	Farnell	9608613
Resistor 240 Ohm	4	Axial	Farnell	6335366
Resistor 10 Ohm (2 watts)	2	Axial	Farnell	9338039
Capacitor 1 uF	4	Axial	Farnell	1161246
Regulator LM317TG	4	T0-220	Farnell	1130736

Decoupling capacitors (placed at all voltage supplies) and connectors (SMA and DC) omitted.

SOT PULSE GENERATOR				
Component	**Qty.**	**Package**	**Retailer / Manufacturer**	**Code**
Pulse Generator				
MOSFET N-channel BSS83 (NXP)	4	SOT-143	Amidata	484-5576
Resistor 330 Ohm	1	SMD 1206	Amidata	740-9091
Matching Stage				
OPAMP AD8009ARZ (Analog Devices)	1	SOIC-8	Amidata	523-7522
OPAMP ADA4857-1YRZ (Analog Devices)	2	SOIC-8	Amidata	759-0207
Resistor 300 Ohm	4	SMD 1206	Amidata	679-2027
Current source				
JFET J107 (Fairchild)	1	TO-92	Farnell	1467946
Resistor 40.2 Ohm	1	SMD 0805	Farnell	1575492
Trimmer 500 Ohm	1	THD Vert. Adjust	Amidata	522-2766
Negative voltage source (x2)				
Charge Pump TC962	1	DIP-8	Microchip	TC962
Electrolytic capacitor 10 uF	2	THD radial	Amidata	116-868
TRANSISTION TIME CONTROL CIRCUIT				
MOSFET N-channel BSS83 (NXP)	2	SOT-143	Amidata	484-5576
MOSFET P-channel BSS84 (NXP)	1	TO-236AB	Amidata	436-8091
JFET P-channel PMBFJ175 (NXP)	1	TO-236AB	Amidata	626-3285
Schottky Diode BAT17 (NXP)	2	SOT-23	Farnell	1081187
Zener 7.5V MMSZ7V5T1G	1	SOD-123	Amidata	544-9781
Capacitor 1 nF	1	SMD 0805	Farnell	1414660
Inverter 74AC14SC	1	SOIC-14	Farnell	1014141
Diode 1N4148 (Fairchild)	1	DO-35	Farnell	9843680
Resistor 300 kOhm	2	SMD 1206	Farnell	1100256
Capacitor 47 pF	1	SMD 0805	Farnell	499160
Current source (x2)				
JFET J107 (Fairchild)	1	TO-92	Farnell	1467946
Resistor 40.2 Ohm	1	SMD 0805	Farnell	1575492
Trimmer 500 Ohm	1	THD Vert. Adjust	Amidata	522-2766
Negative voltage source (x2)				
Charge Pump TC962	1	DIP-8	Microchip	TC962
Electrolytic capacitor 10 uF	2	THD radial	Amidata	116-868

Decoupling capacitors (placed at all voltage supplies) and connectors (SMA and DC) omitted.